

POWER MANAGEMENT

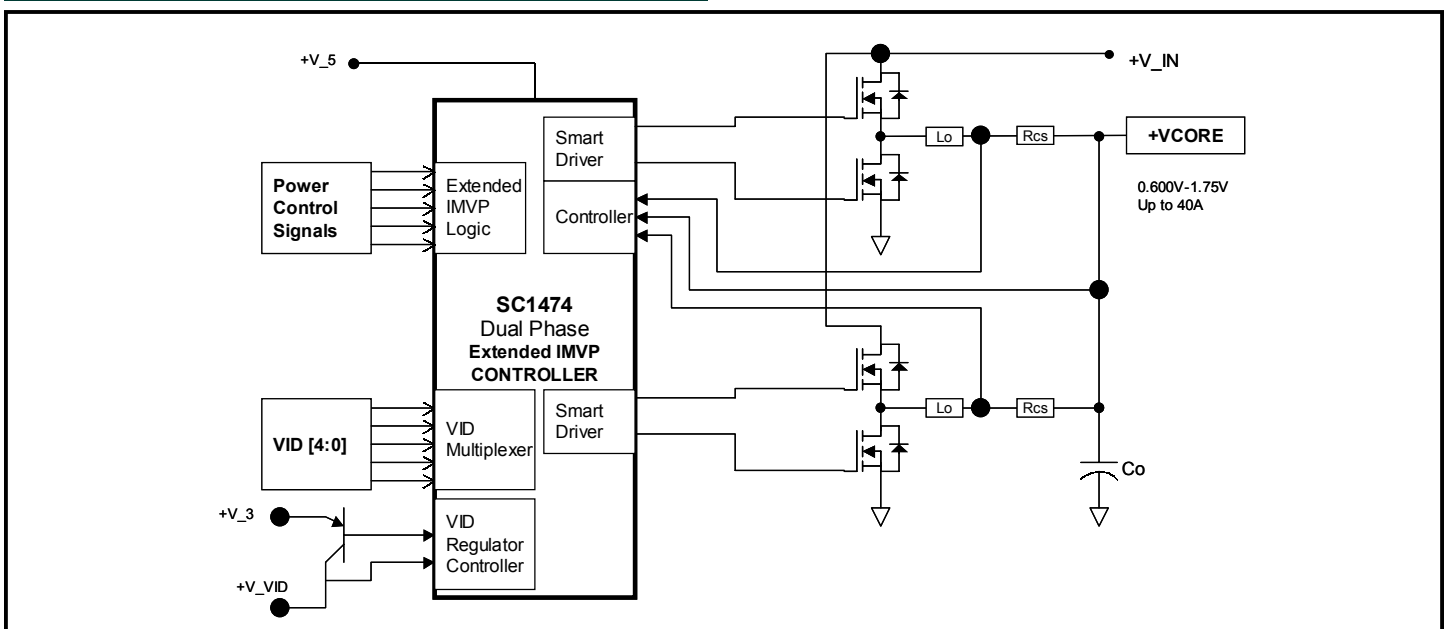
Description

The SC1474 PowerStep III™ IC is a single chip high-performance Hysteretic PWM controller. With dual integrated Smart™ Drivers, it powers advanced Pentium® 4 processors. The SC1474 features extended Intel Mobile Voltage Positioning (IMVP) to increase battery life by reducing the voltage at the processor when it is heavily loaded. It directly supports Intel's SpeedStep™ requirements for even longer battery life. The SC1474 automatically detects performance and battery mode VIDs. In addition, it integrates direct "deeper sleep" mode support. All operating modes incorporate automatic "power-save" to prevent negative current flow in the low-side FET during light loading conditions, saving even more power.

A 5-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements the 0.600V to 1.750V range required by the processor. The hysteretic converter uses a comparator without an error amplifier, and so provides the fastest possible transient response, while avoiding the stability issues inherent to classical PWM controllers. The SC1474 incorporates a controller for V_VID and automatically provides the proper sequencing.

The SC1474 operates from +3.3Vdc Vcca and dual 5V DC drive inputs. It also features soft-start, an open-drain PWRGD signal with power-good blanking, and an enable input. Programmable current limiting latches the SC1474 off after 32 current limit pulses. It comes in a space-saving TSSOP-38 package.

Typical Application Circuit



Features

- ◆ **IMVP3 compliant single chip solution**
- ◆ High speed Dual phase hysteretic controller
- ◆ VID programmable output
- ◆ **Dual integrated 2A/4A drivers**
- ◆ Integrated VID regulator controller
- ◆ Automatic performance/battery mode detection
- ◆ **Dynamic phase current matching**
- ◆ Under-voltage lock out on all Vcc inputs
- ◆ Over-voltage protection on CORE
- ◆ Current Limit protection on CORE
- ◆ Thermal protection
- ◆ Programmable soft-start
- ◆ Powergood flag with blanking during VID changes
- ◆ Automatic powersave at light load
- ◆ 38-pin TSSOP lead free package available. Fully WEEE and RoHS compliant
- ◆ Industrial temperature range

Applications

- ◆ Advanced Intel microprocessors

POWER MANAGEMENT
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Name	Conditions	Min	Max	Units
Supply Voltages	$V_{CCA}, V5_1, V5_2$		-0.3	7	V
Input & Output Voltages	$V_{VDPR}, V_{DPRSL}, V_{VID}[0..4], V_{DAC}, V_{CMPRF}, V_{CMP1,2}, V_{HYS}, V_{CORE}, V_{CL1,2}, V_{CLRF}, V_{PWRGD}, V_{VIDB}, V_{VIDFB}, V_{OSB}, V_{ISH1,2}, V_{SS}, V_{GND}, V_{BG1,2}$		-0.3	$V_{CC} + 0.3$	V
EN	V_{EN}		-0.3	7	V
BST1 to PGND1, BST2 to PGND2		DC	-0.3	40	V
BST1 to PGND1, BST2 to PGND2		Transient, 100ns	-0.3	40	V
BST1 to DRN1			-0.3	7	V
BST2 to DRN2			-0.3	7	V
DRN1 to PGND1, DRN2 to PGND2		DC	-2	35	V
DRN1 to PGND1, DRN2 to PGND2		Transient, 100ns	-4	35	V
TG1 to PGND1			-2	BST1+0.3	V
TG2 to PGND2			-2	BST2+0.3	V
Thermal Resistance Junction to Ambient	θ_{JA}			74	°C/W
Thermal Resistance Junction to Case	θ_{JC}			10	°C/W

Electrical Characteristics

Parameter	Symbol	Conditions	25C			-40C to 125C		Units
			Min	Typ	Max	Min	Max	
Supply (VCCA, V5_1, V5_2, GND)								
V5_1, V5_2 Supply Voltage Range	$V_{5_1, V5_2}$		4.3	5	6	4.3	6	V
VCCA Supply Voltage Range	V_{CCA}		2.9	3.3	5.5	2.9	5.5	V
VCCA Quiescent Current	I_{CCQ}	EN is low			10		10	μ A
		EN is high, and in V_{CCA} or $V5_2$ UVLO		400				
VCCA Operating Current (static)	I_{CC}	When EN is high, not in UVLO, $I_{C_VID_REGULATOR} = 0A$		5			10	mA
Zero Crossing Detector Comparator Offset	V_{OFFSET_ZCD}		-5		8	-5	8	mV
V5_1, V5_2 Quiescent Current	ICCQ_5	$V5_1, V5_2 = 5.0V$		350				μ A

POWER MANAGEMENT
Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	25C			-40C to 125C		Units	
			Min	Typ	Max	Min	Max		
Under Voltage Lock Out Circuits									
V _{CC} A Threshold (falling)	V _{HCCA}		2.7	2.8	2.9	2.7	2.9	V	
V _{CC} A Hysteresis	V _{HYST CCA}			110				mV	
Threshold (V5_1, V5_2 falling)	V _{HV5}		3.9	4.1	4.3	3.9	4.3	V	
V5_1, V5_2 Hysteresis	V _{HYST V5}			240				mV	
V _{VD} Threshold (rising)	V _{VD}		1.04	1.10	1.16	1.04	1.16	V	
VIDFB Hysteresis	V _{VID CC}			300				mV	
Valid VIDFB to CORE regulator starting delay	T _{DELAY_CORE}	C _{SS} = 5nf, V _{CC} A = 3.3V		250				µs	
Enable Input (EN)									
Input high	Ven ih	V _{CC} A = 2.7V -> 3.6V	2			2		V	
		V _{CC} A > 3.6V	0.7*- V _{CC} A						
Input low	Ven il				0.8		0.8	V	
VID Regulator (VIDFB, VIDB)									
Output voltage	V _{VIDRef}	I _C =0 to 650mA, External NPN β _{min} >65	1.164	1.2	1.236	1.164	1.236	V	
Base Drive Output Current	I _{VIDB}		10			10		mA	
VCORE Power Good Generator (PWRGD)									
Input threshold	V _{TH CORE}	V _{DAC} = 0.6 - 1.75V. Note that during UVLO, the output level of this signal is undefined.	upper threshold	1.1*- V _{DAC}	1.12- *V _{DAC}	1.14- *V _{DAC}	1.1*- V _{DA}	1.14*- V _{DAC}	V
			lower threshold	0.9*- V _{DAC}		0.86- *V _{DAC}	0.9*- V _{DAC}	0.86*- V _{DAC}	
			hysteresis		1.2				%
Output Voltage Note that during the latency time of any VID code change, the PWRGD output signal is not valid.	V _{PWRGD}	V _{CORE} = V _{DAC} Pulled-up with external resistor to V _{TT} (1.2V)	0.95- *V _{TT}				0.95*- V _{TT}	V	
		Either V _{CORE} < 0.88*V _{DAC} or V _{CORE} > 1.12*V _{DAC}			0.4		0.4		
		EN is low or EN is high but UVLO condition			0.8		0.8		

POWER MANAGEMENT
Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	25C			-40C to 125C		Units
			Min	Typ	Max	Min	Max	
Core Converter Soft Start (SS)								
V_{SS_CORE} Soft Start Termination Threshold	V_{SS_TERM}		1.575	1.75	1.925	1.575	1.925	V
Core Converter Soft Start Current NOTE Soft Start cap is not discharged until Enable goes low or UVLO cuts in. To enable bias and soft-start, VSSCORE has to drop below V_{SS_EN}	I_{SS}	Charge (Source) Current, $V_{SS_CORE} = 0V$	2.5	4.0	7.0	2.5	7.0	μA
		Discharge (Sink) Current, $V_{SS_CORE} = 1.7V$	5	10		5		mA
V_{SS_CORE} Enable Threshold	V_{SS_EN}			40	100		100	mV
DAC VID[0..4]								
VID Input Threshold	V_{VID_IH}	$V_{CC_A} = 2.7V \rightarrow 3.6V$	2			2		V
		$V_{CC_A} > 3.6V$	0.7*			0.7*-	V_{CC_A}	
	V_{VID_IL}				0.8		0.8	
VID Input -pull-up Current, VID[0..4]	I_{VID}	VID[0..4] = 00000 ... 11111		10		4	16	μA
DAC Output Voltage Accuracy	V_{DAC_ERR}	$0 < T_A < 125\text{ }^\circ C$ $R_{DAC} = 50k\Omega$ VID[0..4] = 00000 ... 10110	-0.85		+0.85	-0.85	+0.85	%
		$-40 < T_A < 125\text{ }^\circ C$ $R_{DAC} = 50k\Omega$ VID[0..4] = 00000 ... 10110	-1.5		+1.5	-1.5	+1.5	
		VID[0..4] = 10111 ... 11111	-2.0		+2.0	-2.0	+2.0	

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Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	25C			-40C to 125C		Units
			Min	Typ	Max	Min	Max	
Deeper Sleep								
Input Offset Voltage	$ V_{VDPR} - V_{DAC} $	$V_{VDPR} = 0.85V$		$ \pm 1 $			$ \pm 3 $	%
CORE Comparator (CMP1, CMP2, CMPRF, HYS)								
Input Bias Current	I_{CMPRF}	$V_{CMP} = V_{CMPRF} = 1.3V$			$ \pm 2 $		$ \pm 2 $	μA
Input Offset Voltage	$ V_{CMP1,2} - V_{CMPRF} $	$V_{CMPRF} = 1.3V$		$ \pm 1.5 $	$ \pm 3 $		$ \pm 3 $	mV
Hysteresis Setting Current Performance Mode $I_{CMP} = 0$	$R_{HYS} = 17\text{ k}\Omega$	$V_{CMP} < V_{CMPRF}$	90	100	110	90	110	μA
		$V_{CMP} > V_{CMPRF}$	-6		+6	-6	+6	
	$R_{HYS} = 170\text{ k}\Omega$	$V_{CMP} < V_{CMPRF}$	7	10	13	7	13	
		$V_{CMP} > V_{CMPRF}$	-2		+2	-2	+2	
Hysteresis Setting Current Battery Mode $I_{CMP} = 0$	$R_{HYS} = 17\text{ k}\Omega$	$V_{CMP} < V_{CMPRF}$	68	80	92	68	92	μA
		$V_{CMP} > V_{CMPRF}$	-6		+6	-6	+6	
	$R_{HYS} = 170\text{ k}\Omega$	$V_{CMP} < V_{CMPRF}$	5.6	8	10.4	5.6	10.4	
		$V_{CMP} > V_{CMPRF}$	-2		2	-2	2	
Current Sharing (ISH1, ISH2, CMP1)								
I_{SHARE} Enable Threshold			0.3	0.4	0.5	0.3	0.5	V
Amplifier Offset			-3		+3	-3	3	mV
I_{SHARE} Current Range			12	20	27	12	27	%Ihys

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Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	25C			-40C to 125C		Units	
			Min	Typ	Max	Min	Max		
Current Limit Comparator (CL1, CL2, CLRF)									
Input Bias Current	$ \pm I_{CL1,2} $	$V_{CL} = 1.3V$				$ \pm 5 $		$ \pm 5 $	μA
Current Limit Setting Current Performance Mode	$ \pm I_{CLRF} $	$R_{HYS} = 17\text{ k}\Omega$	$V_{CLRF} - V_{CL} = -10mV$	225	250	275	225	275	μA
			$V_{CLRF} - V_{CL} = 10mV$	270	330	330	270	330	
		$R_{HYS} = 170\text{ k}\Omega$	$V_{CLRF} - V_{CL} = -10mV$	20	25	30	20	30	
			$V_{CLRF} - V_{CL} = 10mV$	23	30	37	23	37	
Current Limit Setting Current Battery Mode	$ \pm I_{CLRF} $	$R_{HYS} = 17\text{ k}\Omega$	$V_{CLRF} - V_{CL} = -10mV$	180	200	220	180	220	μA
			$V_{CLRF} - V_{CL} = 10mV$	216	240	264	216	264	
		$R_{HYS} = 170\text{ k}\Omega$	$V_{CLRF} - V_{CL} = -10mV$	16	20	24	16	24	
			$V_{CLRF} - V_{CL} = 10mV$	19	24	29	19	29	
Input Offset Voltage	$ V_{CL1,2} - V_{CLRF} $	$V_{CLRF} = 1.3V$			$ \pm 4 $	$ \pm 6 $		$ \pm 6 $	mV
High-Side Drivers (TG1, TG2)									
Peak Output Current	I_{pkh}			2					A
Output Resistance	R_{SRC}	$I = 100mA, V5_1, V5_2 = 5.0V, V_{BST} = 5.0V$		1	3		3		Ω
	R_{SINK}			1	3		3		
Rise Time	tr_{TG}	$CL = 3nF, V_{BST} - V_{DRN} = 5V$		15	24		24		ns
Fall Time	tf_{TG}			15	24		24		ns
Propagation Delay, TG going High ⁽²⁾		CMP crossing CMPRF to 10% point of TG, $C_{TG} = 3nF, BG = 0V$		37					ns
Propagation Delay, TG going Low ⁽²⁾		CMP crossing CMPRF to 90% point of TG, $C_{TG} = 3nF, DRN = 0V$		41					ns

POWER MANAGEMENT
Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	25C			-40C to 125C		Units
			Min	Typ	Max	Min	Max	
Low-Side Driver (BG1, BG2)								
Peak Output Current	I_{pk}			4				A
Output Resistance	R_{SRC}	$I = 100mA, V_{5_1}, V_{5_2} = 5.0V$		1	3		3	Ω
	R_{SINK}			0.5	2		2	
Rise Time	$t_{r_{BG}}$	$CI = 3nF, V_{V5} = 5V$		15	24		24	ns
Fall Time	$t_{f_{BG}}$			10	17		17	ns
Propagation Delay, BG going High ⁽²⁾		CMP crossing CMPRF to 10% point of BG, $C_{BG} = 3nF, DRN = 0V$		32				ns
Propagation Delay, BG going Low ⁽²⁾		CMP crossing CMPRF to 90% point of BG, $C_{BG} = 3nF$		27				ns
On Resistance	R_{on-OSB}	OSB switch		35			100	Ω
Drivers (TG1, TG2, BG1, BG2)								
Shoot-thru Protection Delay Time ⁽²⁾			35	50	65			ns

Note:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

(2) Guaranteed by design.

POWER MANAGEMENT
Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Description
6	DPRSL	Deeper Sleep signal. In deeper sleep, the DAC output is set by the VDPR pin.
7	OSB	Offset Battery. This is an open-drain output. When in battery mode, this is driven low impedance to ground of less than 100Ω.
8	HYS	Core Comparator Hysteresis. Connects to ground is an external resistor, called RHYS. In performance mode, Hysteresis current is established by an internal V_{REF} voltage, 1.7V, divided by R_{HYS} . In battery mode, the Hysteresis current is 80% of V_{REF} / R_{HYS} .
9	VDPR	The voltage on this pin sets the DAC output during Deeper Sleep.
10	VID4	VID most significant bit main controller voltage programming DAC input.
11	VID3	VID input
12	VID2	VID input
13	VID1	VID input
14	VID0	VID least significant bit main controller voltage programming DAC input.
15	SS	Soft Start. An external cap defines the soft start ramp multiplexed between VID regulator and CORE regulator.
16	PWRGD	Power Good - open drain output. When the Main Converter Output approaches and stays within $\pm 12\%$ of the VID_DAC setting, and the soft-start period has terminated, this signal is pulled high by an external resistor.
17	BST2	Bootstrap pin for phase 2. A capacitor is connected between BST2 and DRN2 pins to develop the floating bootstrap voltage for the high-side MOSFET.
18	TG2	Output gate drive for the phase 2 switching (high-side) MOSFET.
19	DRN2	This pin connects to the junction of the phase 2 switching and synchronous MOSFETs.
20	V5_2	5V supply for phase 2. Connect a 1mF ceramic capacitor as close as possible from V5_2 to PGND2.
21	BG2	Output drive for the phase 2 synchronous (low-side) FET.
22	PGND2	Power ground for phase 2. Connect to the synchronous FET power ground.
23	CORE	Main CORE Converter Output Feedback to the power-good generator. A small RC filter should be used to filter out any HF component to prevent faulty trip condition.
24	DAC	Main controller Digital-to-Analog Output.
25	GND	Ground.
26	ISH2	Driver 2 current sharing filter pin.
27	CL2	Current Limit Input Pin for phase 2.
28	CMP2	Core Comparator input pin for phase 2.
29	CMPRF	Shared Core Comparator Reference input pin.
30	VCCA	3.3V or 5V supply for precision analog circuitry.

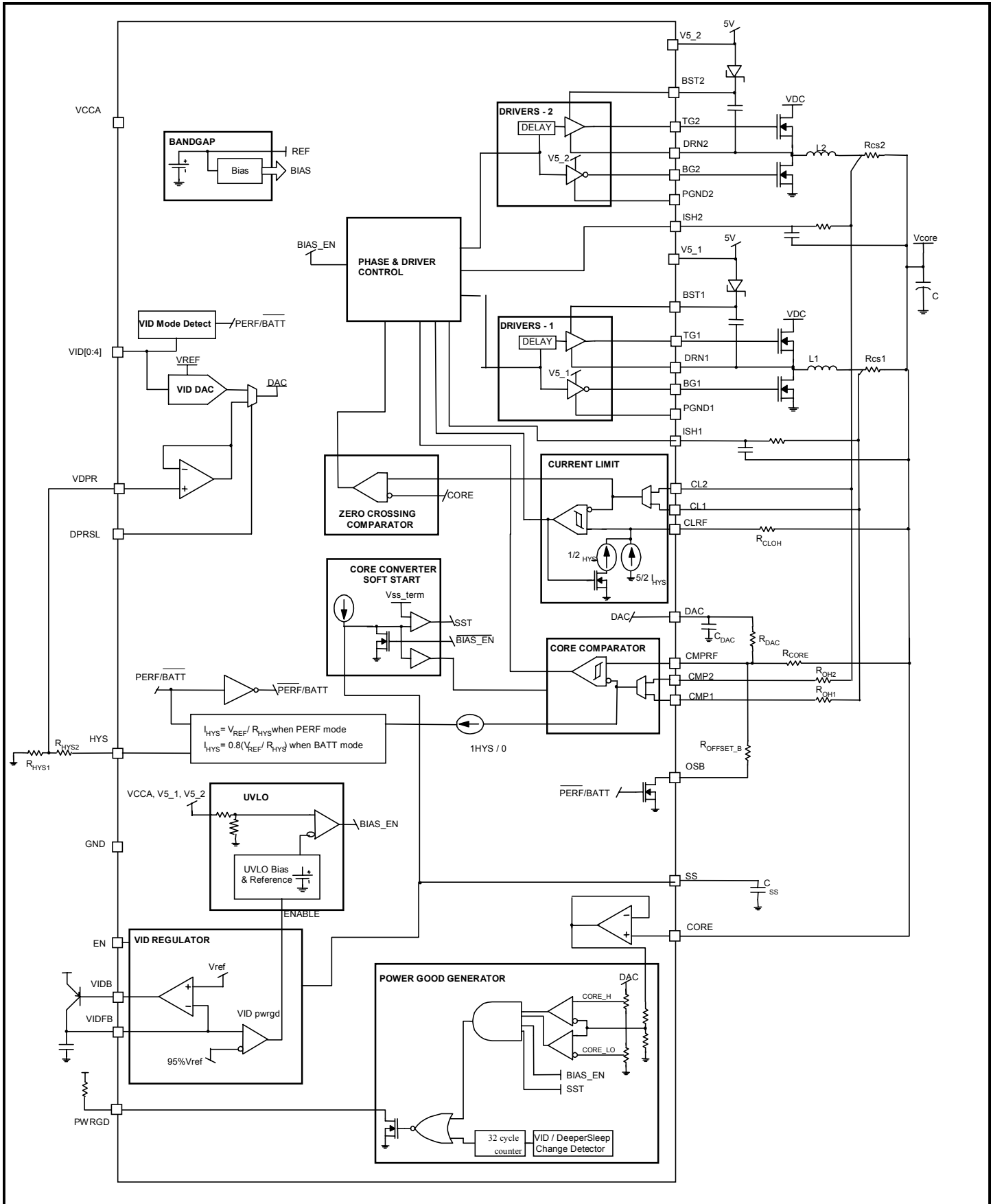
POWER MANAGEMENT

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Description
31	CLRF	Shared Current Limit Reference Input Pin.
32	CMP1	Core Comparator input pin for phase 1.
33	CL1	Current Limit Input Pin for phase 1.
34	ISH1	Driver 1 current sharing filter pin. Pull this pin to ground to disable Active Current Sharing.
35	EN	Enable - active high. This is capable of accepting a 5.0V signal level.
36	PGND1	Power ground for phase 1. Connect to the synchronous FET power ground.
37	BG1	Output drive for the phase 1 synchronous (low-side) FET.
38	V5_1	5V supply for phase 1. Connect a 1mF ceramic capacitor as close as possible from V5_1 to PGND1.

POWER MANAGEMENT

Block Diagram



POWER MANAGEMENT
Applications Information
SUPPLY, BIAS, UVLO, POWERGOOD GENERATOR
Supplies

The SC1474 is optimized to operate from a $3.3\text{ V} \pm 5\% V_{\text{CCA}}$ but also works up to a 6V maximum. We recommend using 3.3V for V_{CCA} in a processor power application because the VID inputs are internally pulled up to V_{CCA} . Using a higher voltage may result in an overvoltage on the processor VID inputs. The driver power inputs (V_{5_1} and V_{5_2}) are designed for a $5\text{ V} \pm 10\%$ input.

Under Voltage Lock-Out Circuit

The Under-Voltage-Lock-Out Circuit consists of comparators which monitor the V_{CCA} , V_{5_1} , and V_{5_2} voltage levels. The SC1474 enters UVLO mode when any of the supplies has not ramped above the upper threshold or has dropped below the lower threshold. In addition, the CORE regulator is disabled until the VID regulator exceeds its threshold. In UVLO mode, the VID regulator is shut down and the gate drives are tri-stated.

Power Good Generator

If the chip is enabled but not in UVLO condition, and the core voltage gets within $\pm 12\%$ (nominal) of the VID programmed value, then a high level Power Good signal is generated on the PWRGD pin to trigger the processor power up sequence. If the chip is either disabled or enabled but in UVLO condition, then PWRGD is undefined. This is an open-drain output and will be pulled-up externally by a 680Ω or larger resistor.

During soft start, PWRGD stays low independently from the status of Vcore voltage. During VID code change latency time or a DeeperSleep transition, PWRGD is forced high (open drain) by logic circuits. PWRGD resumes normal functioning after 32 clock cycles.

Over-voltage Protection

If the CORE voltage is greater than +12% of the DAC (i.e. out of the powergood window), the SC1474 will latch off and hold the low-side driver on permanently. Either the power or EN must be recycled to clear the latch. The latch is disabled during softstart and VID/DeeperSleep transitions. For safety, the latch is enabled if the CORE voltage exceeds 2V even during VID/DeeperSleep transitions.

Thermal Shutdown

The device will be disabled when the internal junction temperature reaches approximately 160C and will not re-start until the temperature has dropped by about 10C.

Band Gap Reference

A $\pm 0.85\%$ precision Band Gap Reference acts as the internal reference voltage standard of the chip, which all critical biasing voltages and currents are derived from. All references to V_{REF} in the equations to follow use $V_{\text{REF}}=1.7\text{V}$.

CORE CONVERTER CONTROLLER
Precision VID DAC Reference

This 5-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by either CMOS logic level VID code applied to the DAC inputs. The VID code vs. the DAC output is shown in table 5 below. The accuracy of the VID DAC is maintained on the same level as of the Band Gap Reference.

VID					V_{CC}	VID					V_{CC}
4	3	2	1	0	V	4	3	2	1	0	V
0	0	0	0	0	1.750	1	0	0	0	0	0.975
0	0	0	0	1	1.700	1	0	0	0	1	0.950
0	0	0	1	0	1.650	1	0	0	1	0	0.925
0	0	0	1	1	1.600	1	0	0	1	1	0.900
0	0	1	0	0	1.550	1	0	1	0	0	0.875
0	0	1	0	1	1.500	1	0	1	0	1	0.850
0	0	1	1	0	1.450	1	0	1	1	0	0.825
0	0	1	1	1	1.400	1	0	1	1	1	0.800
0	1	0	0	0	1.350	1	1	0	0	0	0.775
0	1	0	0	1	1.300	1	1	0	0	1	0.750
0	1	0	1	0	1.250	1	1	0	1	0	0.725
0	1	0	1	1	1.200	1	1	0	1	1	0.700
0	1	1	0	0	1.150	1	1	1	0	0	0.675
0	1	1	0	1	1.100	1	1	1	0	1	0.650
0	1	1	1	0	1.050	1	1	1	1	0	0.625
0	1	1	1	1	1.000	1	1	1	1	1	0.600

On start-up, the VID Management circuit assumes the initial VID code is for Performance Mode. The hysteresis current values and OSB switch are set accordingly. On a VID code change, the VID Management performs a binary comparison of the current and new VID codes. If the new code represents a higher voltage than the current code, the mode is set to Performance. If the new code represents a lower voltage, the mode is set to Battery.

Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of about 20ns at a 20mV overdrive. Its hysteresis is determined by the ratio of the high accuracy internal reference voltage, V_{REF} , divided by R_{HYS} when in Performance Mode. In Battery Mode, the hysteresis current is 80% of this ratio.

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Applications Information (Cont.)

Current Limit Comparator

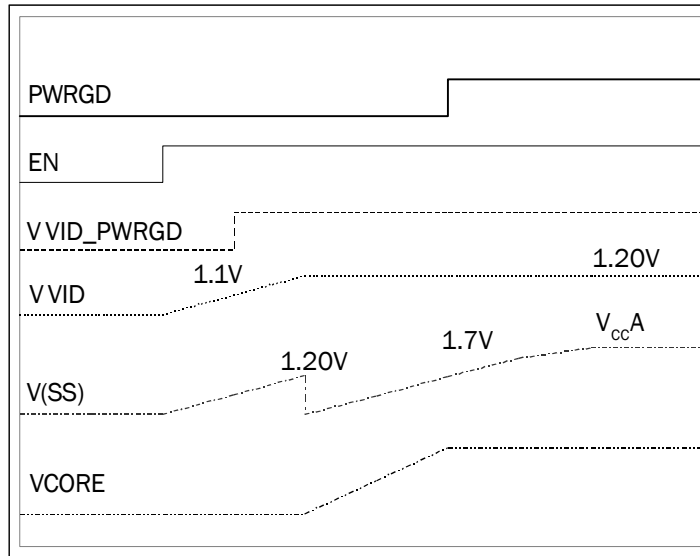
The Current Limit Comparator monitors the core converter output current in each phase and turns the high side switch off when the current in either phase exceeds the upper current limit threshold, V_{HCL} and re-enabled only if the load current drops below the lower current limit threshold, V_{LCL} . The current is sensed by monitoring the voltage drop across the current sense resistor, R_{CS} connected in series with the core converter inductor (the same resistor used for DSPS input signal generation)

Current limit Latch

If the CORE voltage goes lower than 12% below the VID (i.e. out of the powergood window), then sustained current limiting (32 current limit pulses) will cause the part to permanently latch off. The latch is inhibited during soft-start.

Core Converter Soft Start Timer

This block first controls the ramp-up time of the VID voltage, then sets the delay time before the CORE voltage begins its ramp. Finally, the CORE voltage ramp time is defined. The primary purpose is to reduce the initial in-rush current on the core input voltage (battery) rail.



VID TRANSITIONING

Powergood blanking

On any VID change or DeeperSleep change, the PowerGood signal is blanked for 32 CO cycles (approx. 100us) to prevent glitching on the PowerGood during the transition.

Performance/Battery Mode

In Battery Mode, the hysteresis current (for CORE and Current Limit) is set to 80% of its nominal value. At the same time, the OSB pin is pulled low. In Performance Mode, the OSB pin is high impedance and the hysteresis current operates at 100%.

Battery/Performance Mode is automatically determined by comparing old and new VID codes during a VID transition. The lower code (higher Vcore setting) is determined to be Performance Mode. The SC1474 starts up in Performance Mode.

Deeper Sleep function

When DPRSL is high, the DAC is set by the voltage on the VDPR pin. On a DPRSL transition, the PWGD pin is forced high (blanked) for 32 CO cycles. The OSB offset is disabled during Deeper Sleep.

Power-Save

A zero-crossing comparator detects when the current thru the external sense resistor reverses. At this point, the bottom FET is latched off. The latch is reset when the controller decides to switch on the top FET. This prevents excessive switching at light loads and hence saves switching power losses.

VID Regulator

The VID regulator along with an external PNP provides a 1.2V supply at up to 650mA. The CORE regulator is not allowed to start until the VID regulator has exceeded its threshold for a period of time defined by the external Soft Start capacitor.

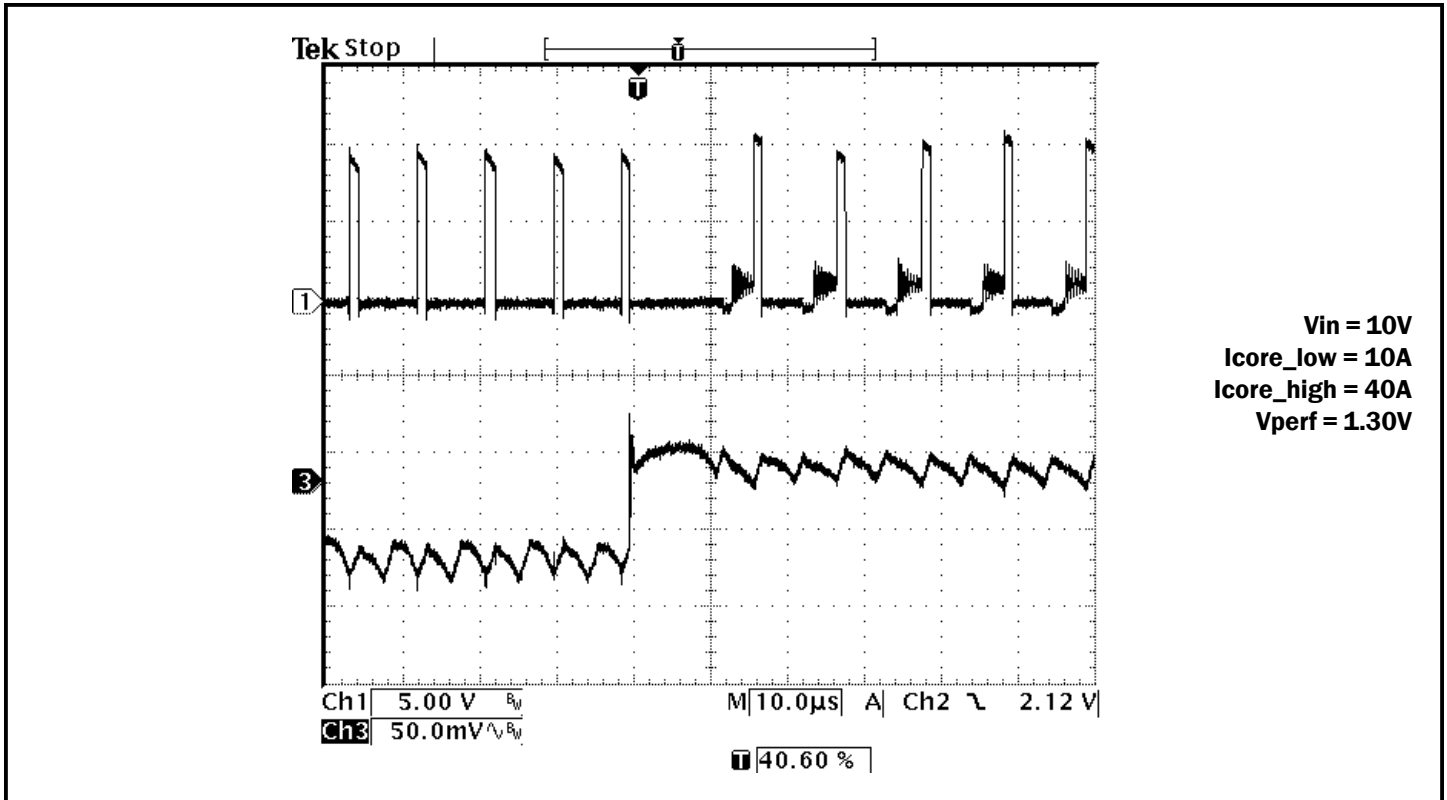
Dynamic Current Sharing

The average current in each phase is compared and the controller dynamically alters the switching set-points to match the currents.

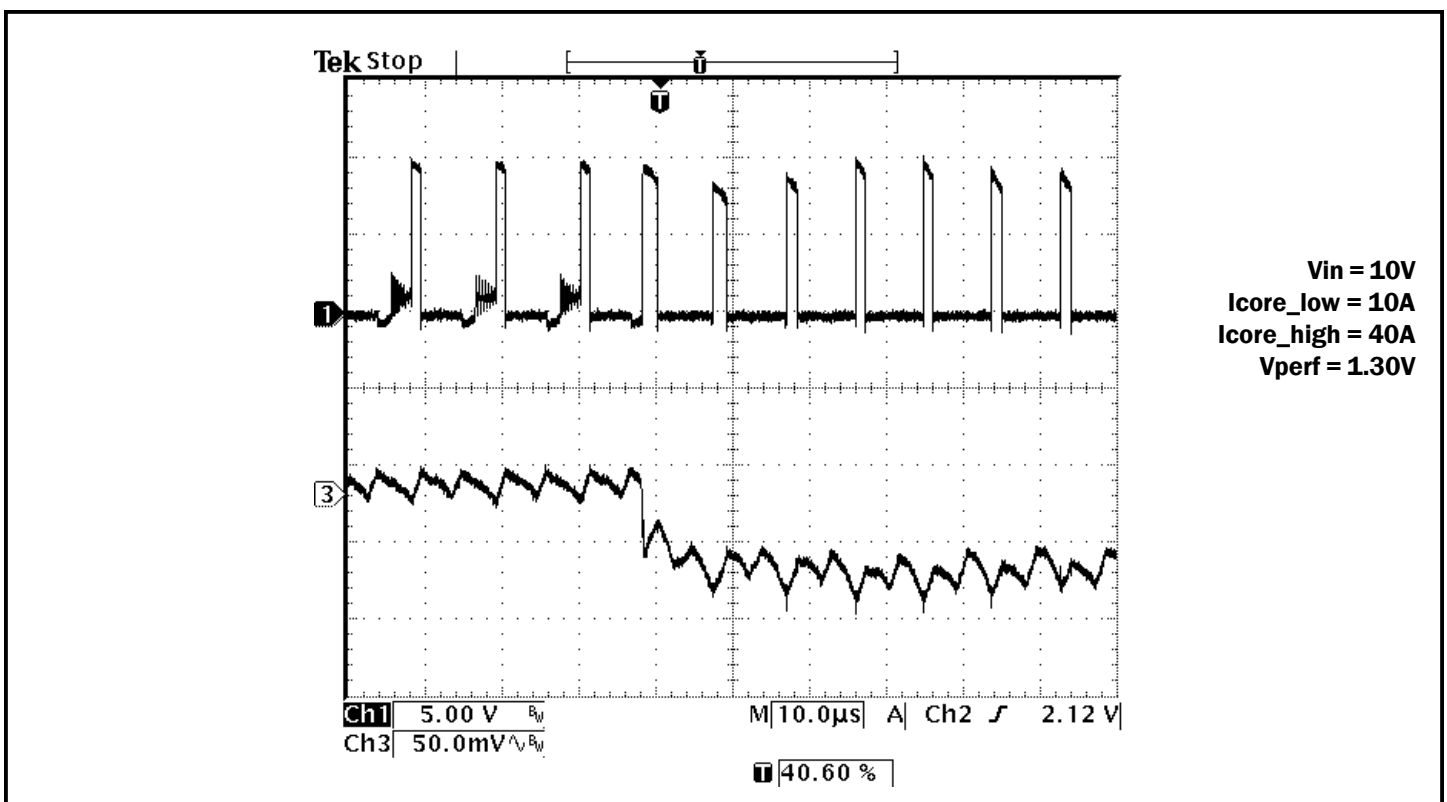
POWER MANAGEMENT

Typical Characteristics

Performance mode dynamic load release response



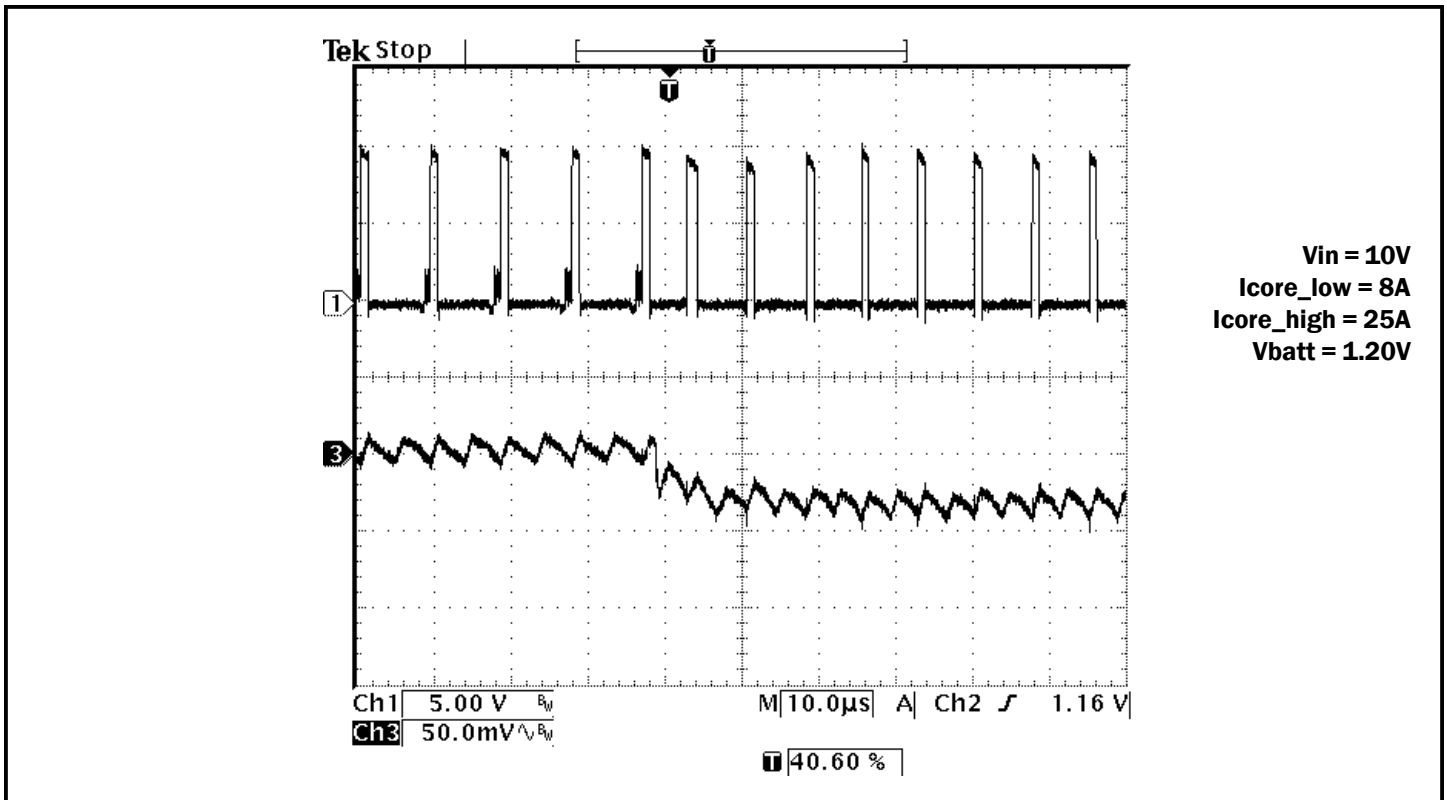
Performance mode dynamic load response



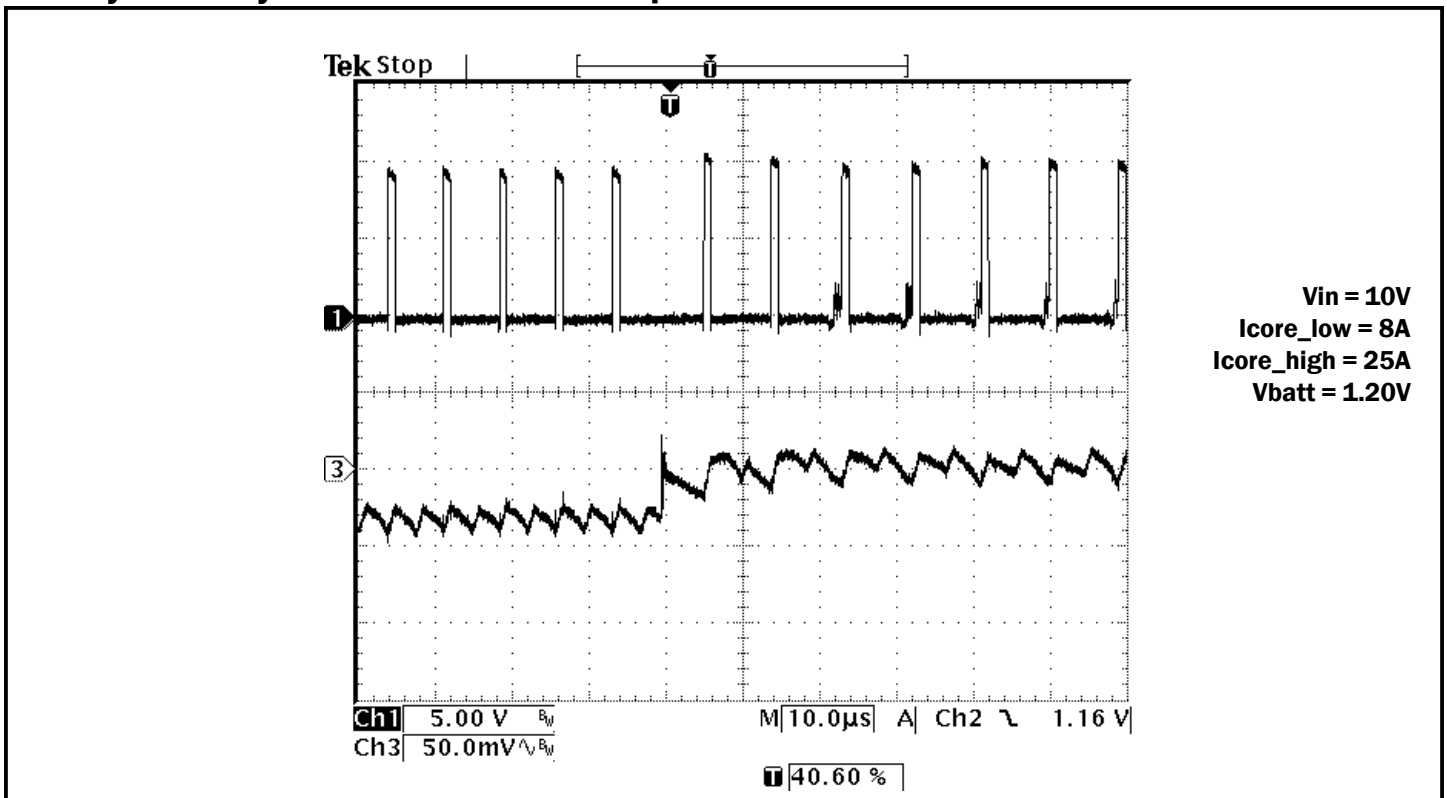
POWER MANAGEMENT

Typical Characteristics (Cont.)

Battery mode dynamic load response



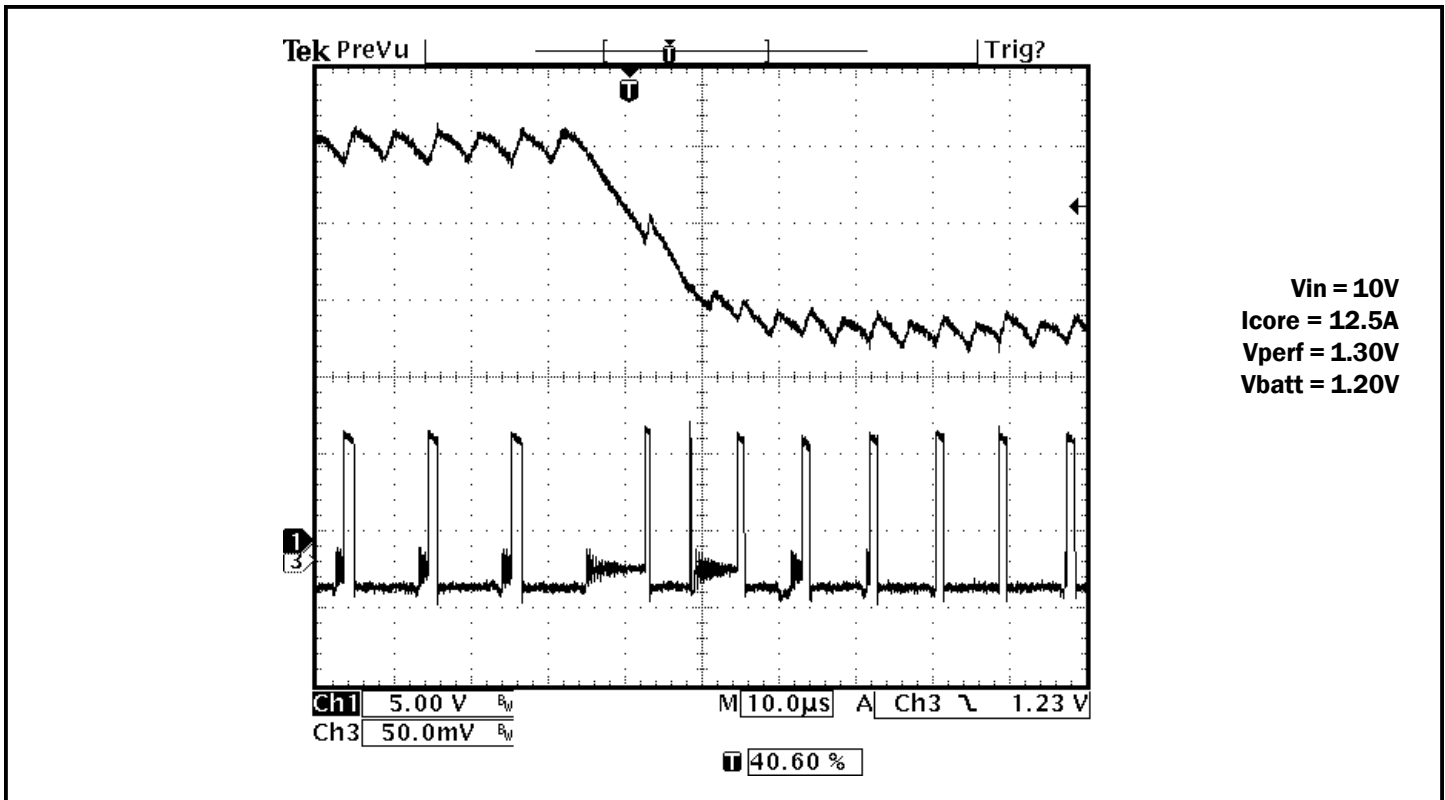
Battery mode dynamic load release response



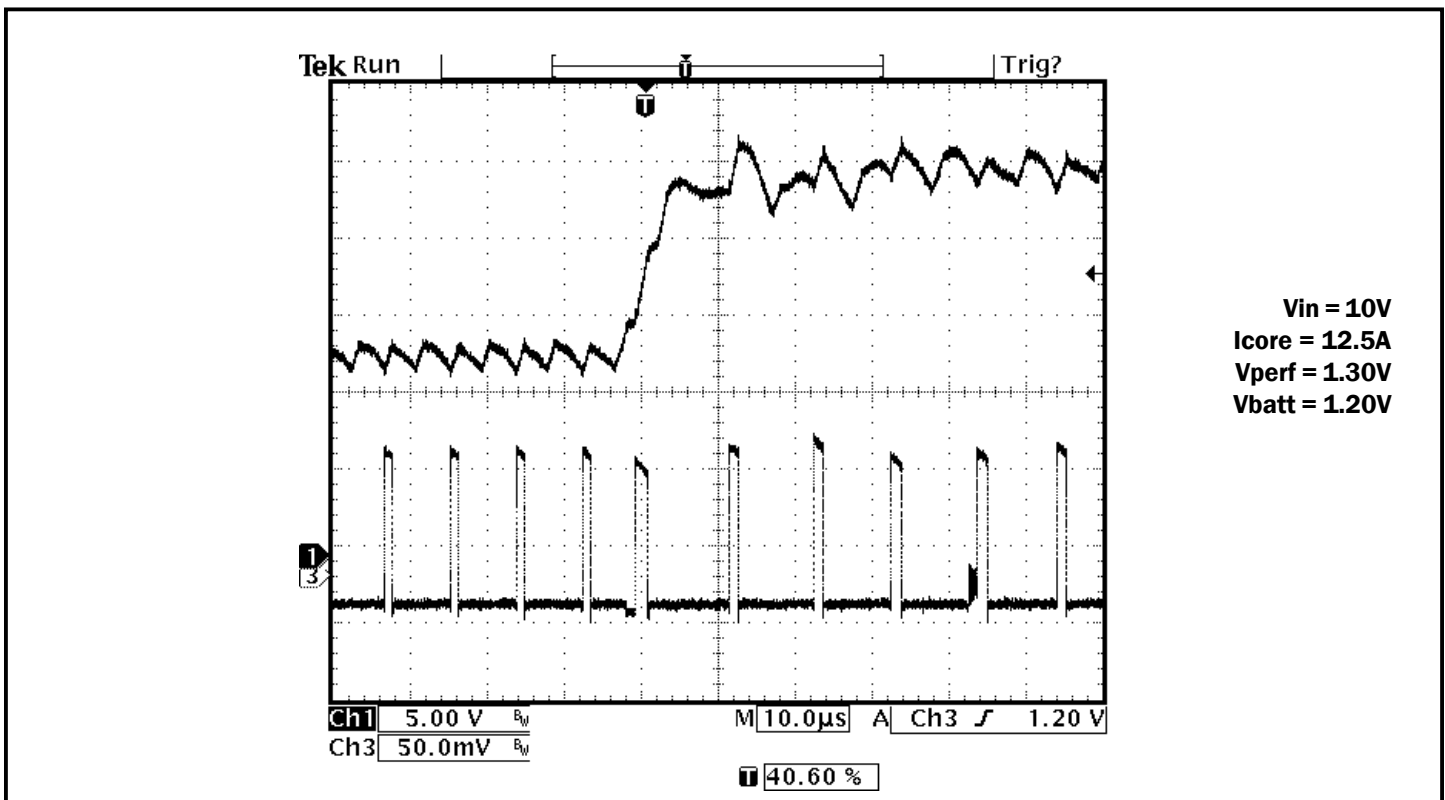
POWER MANAGEMENT

Typical Characteristics (Cont.)

Performance mode to Battery mode transition



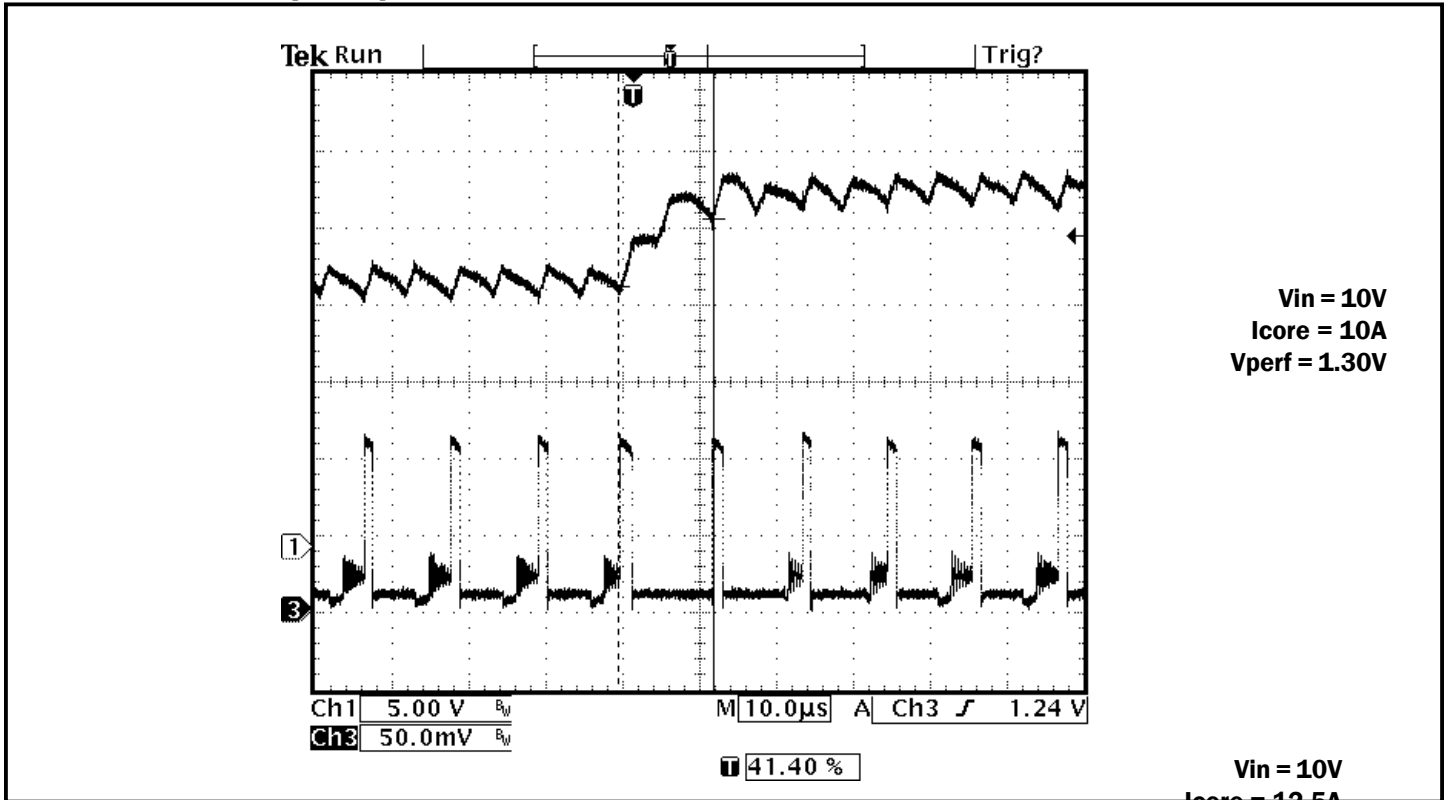
Performance mode to Battery mode transition



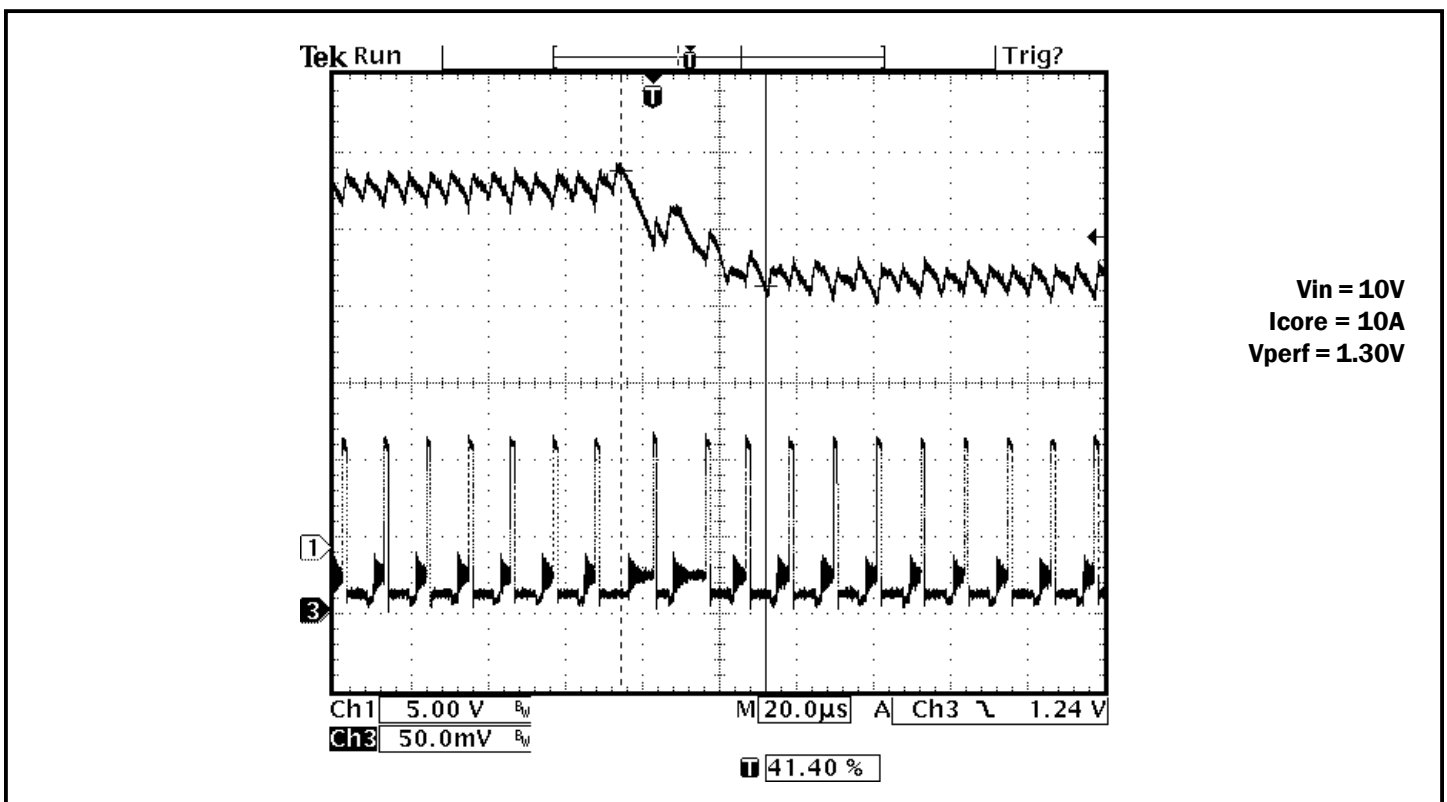
POWER MANAGEMENT

Typical Characteristics (Cont.)

Performance Deepsleep mode to Performance mode transition



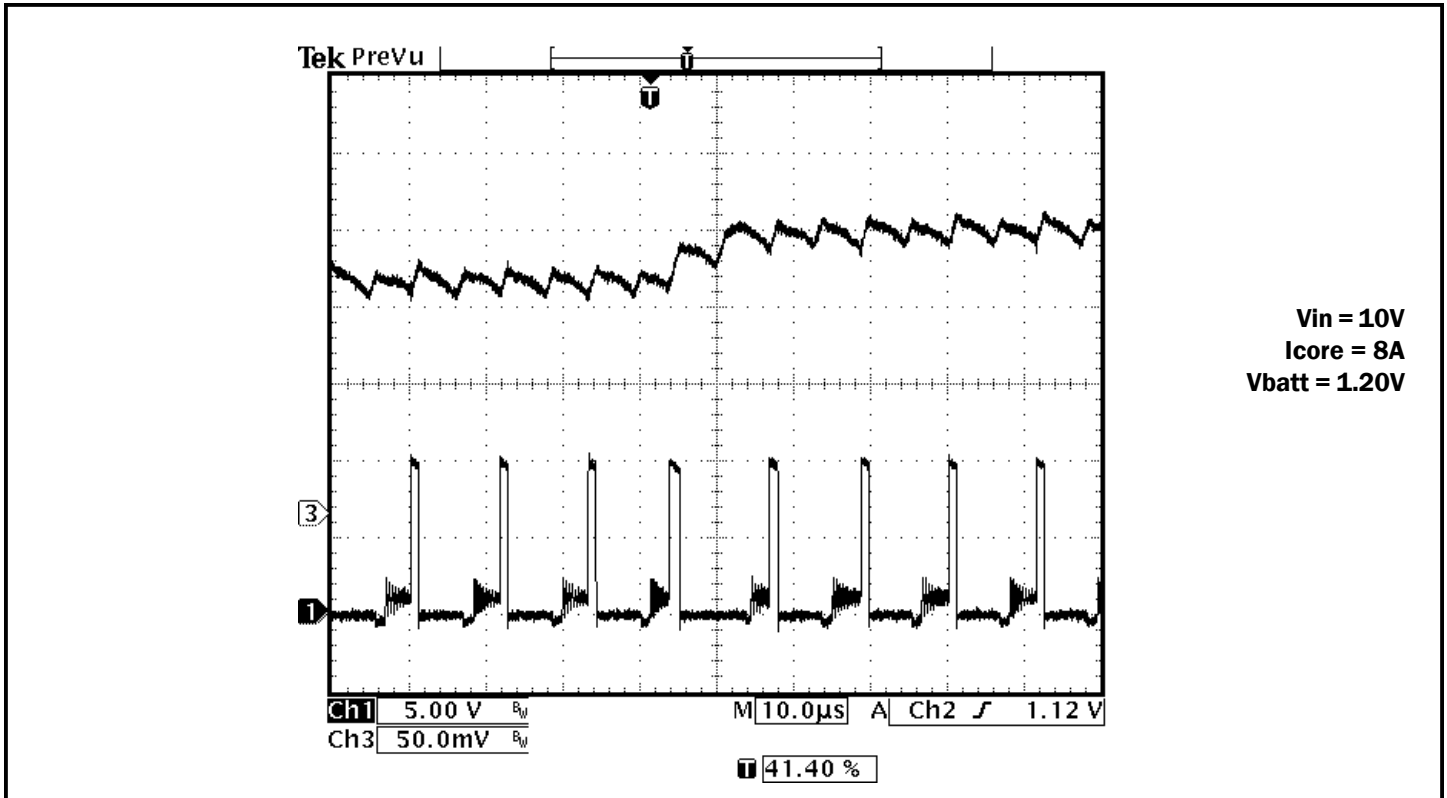
Performance mode to Performance Deepsleep mode transition



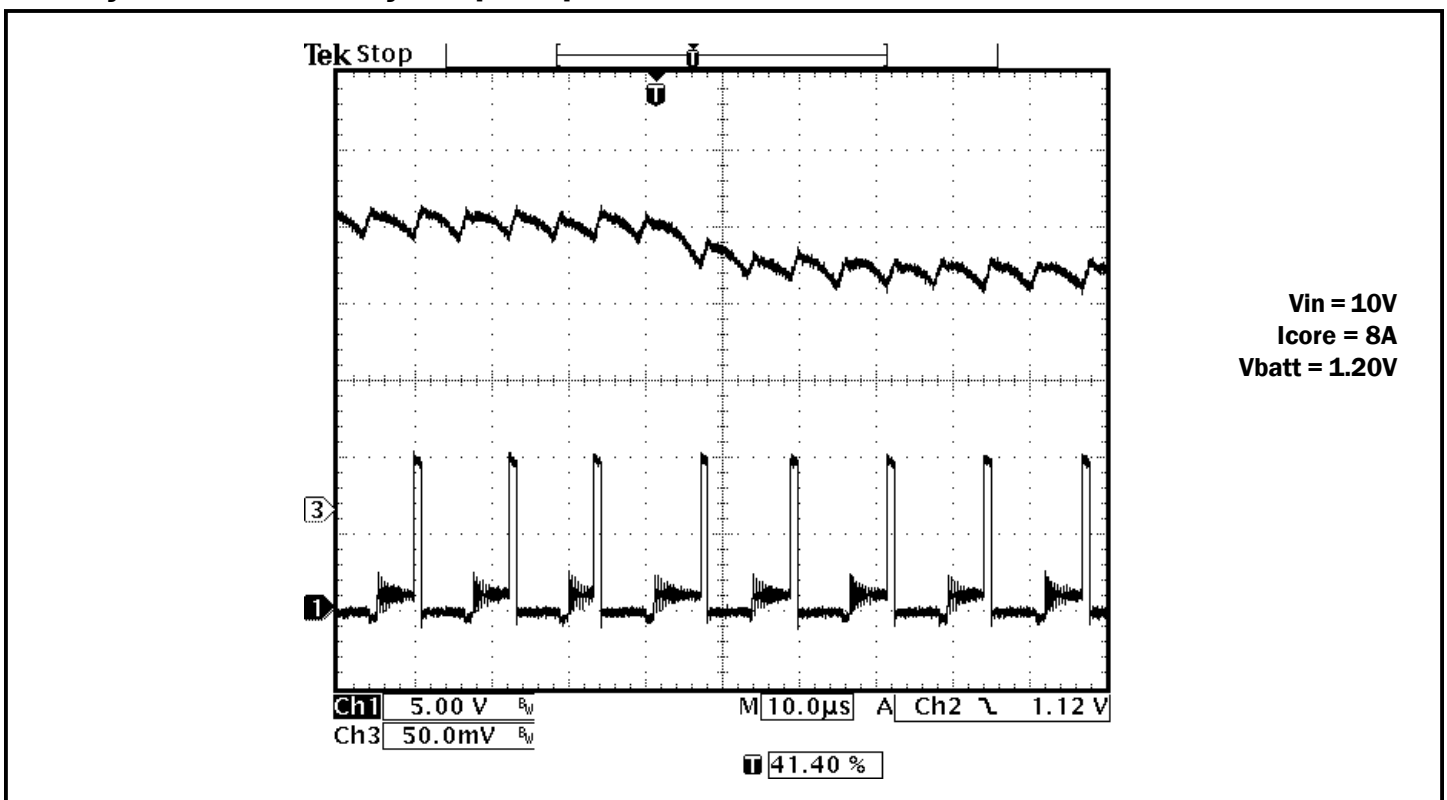
POWER MANAGEMENT

Typical Characteristics (Cont.)

Battery deepsleep mode to Battery mode transition



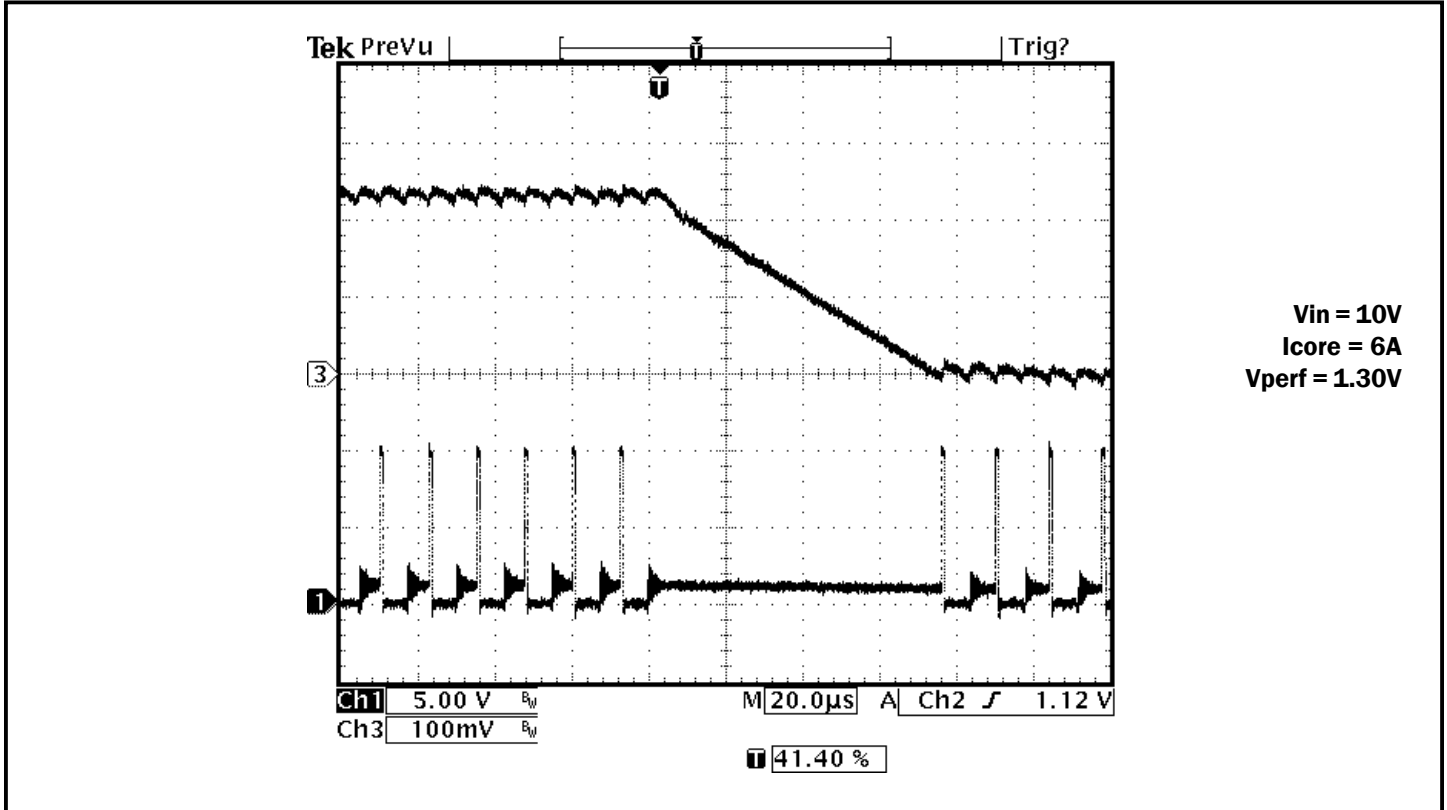
Battery mode to Battery deepsleep mode transition



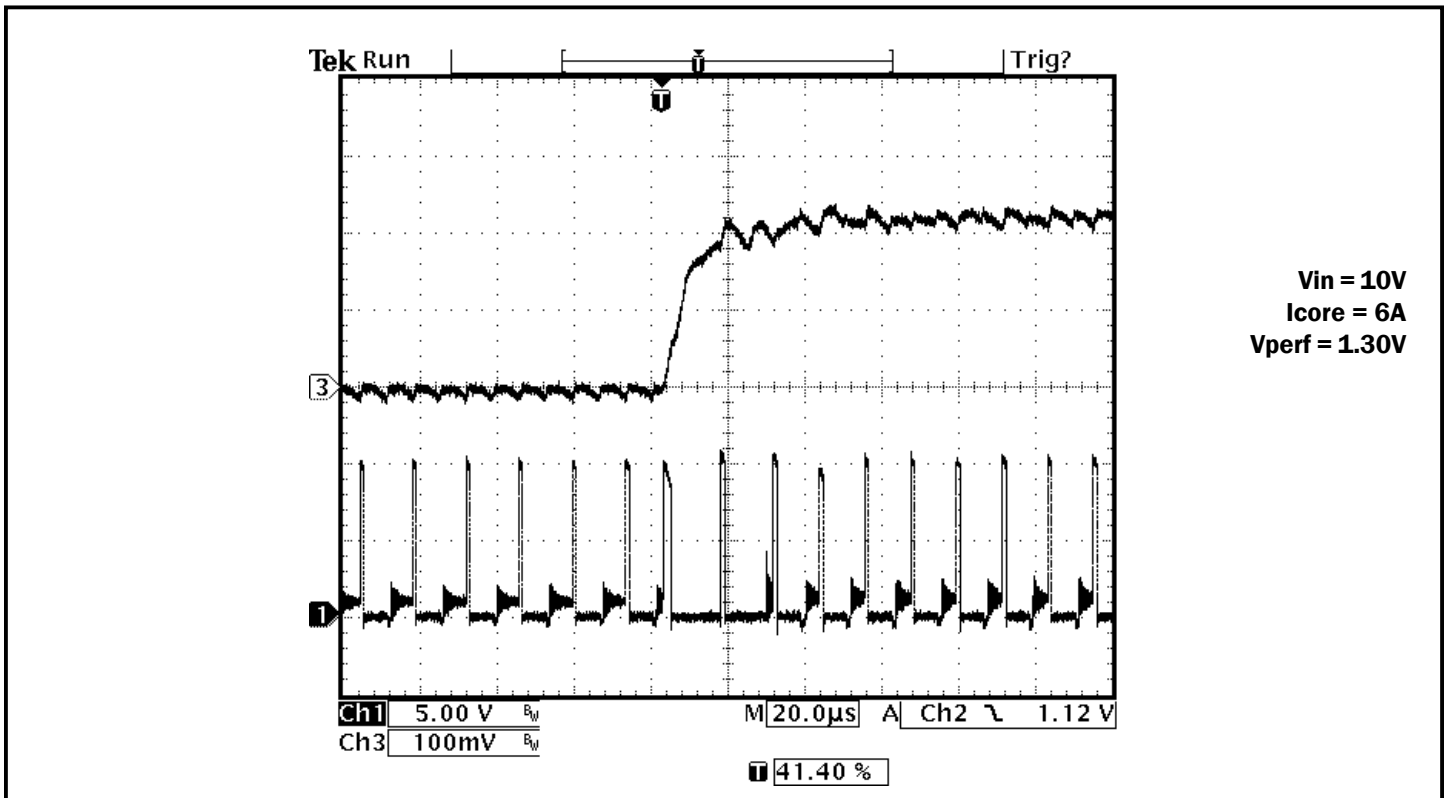
POWER MANAGEMENT

Typical Characteristics (Cont.)

Performance deepsleep mode to Deepsleep mode transition



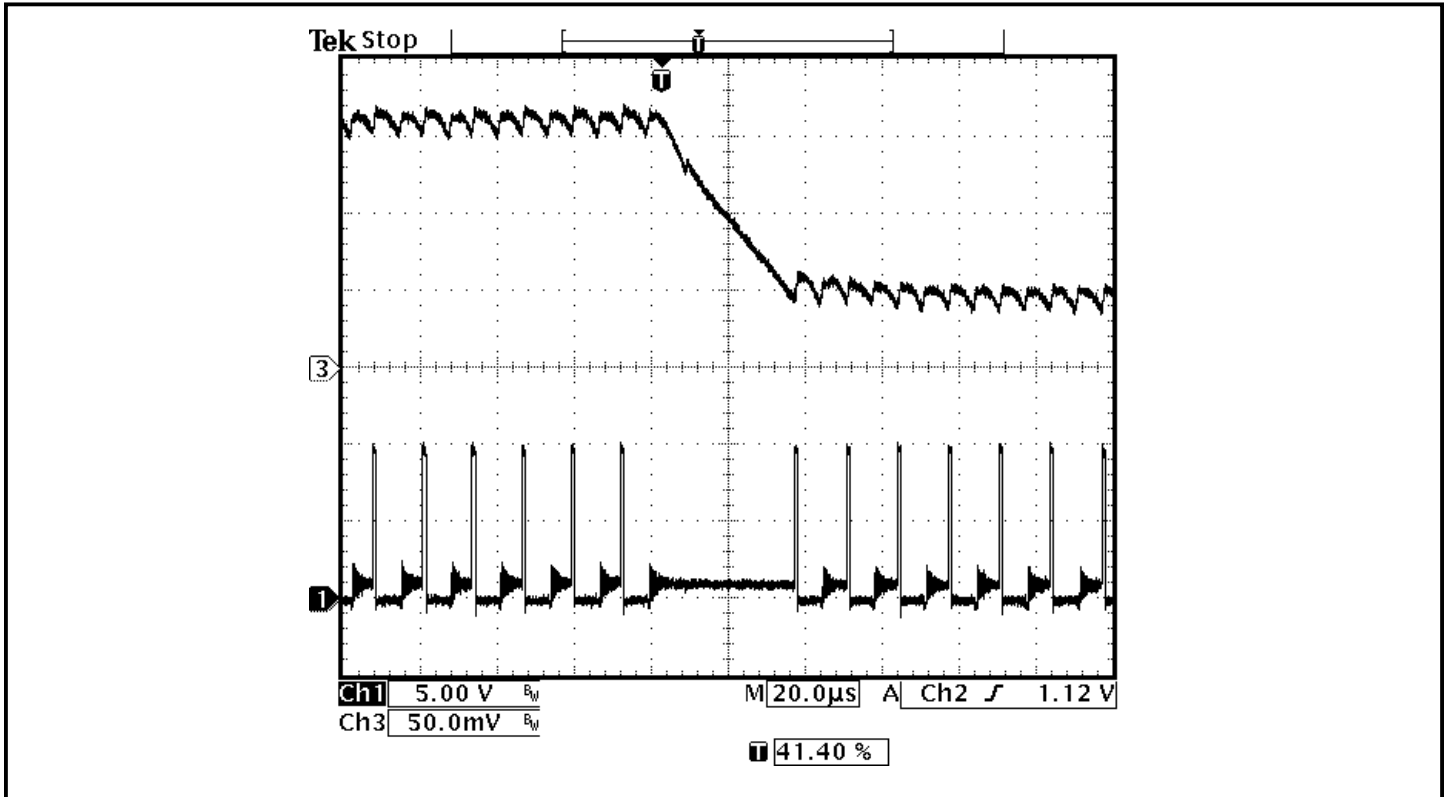
Deepsleep mode to Performance deepsleep mode transition



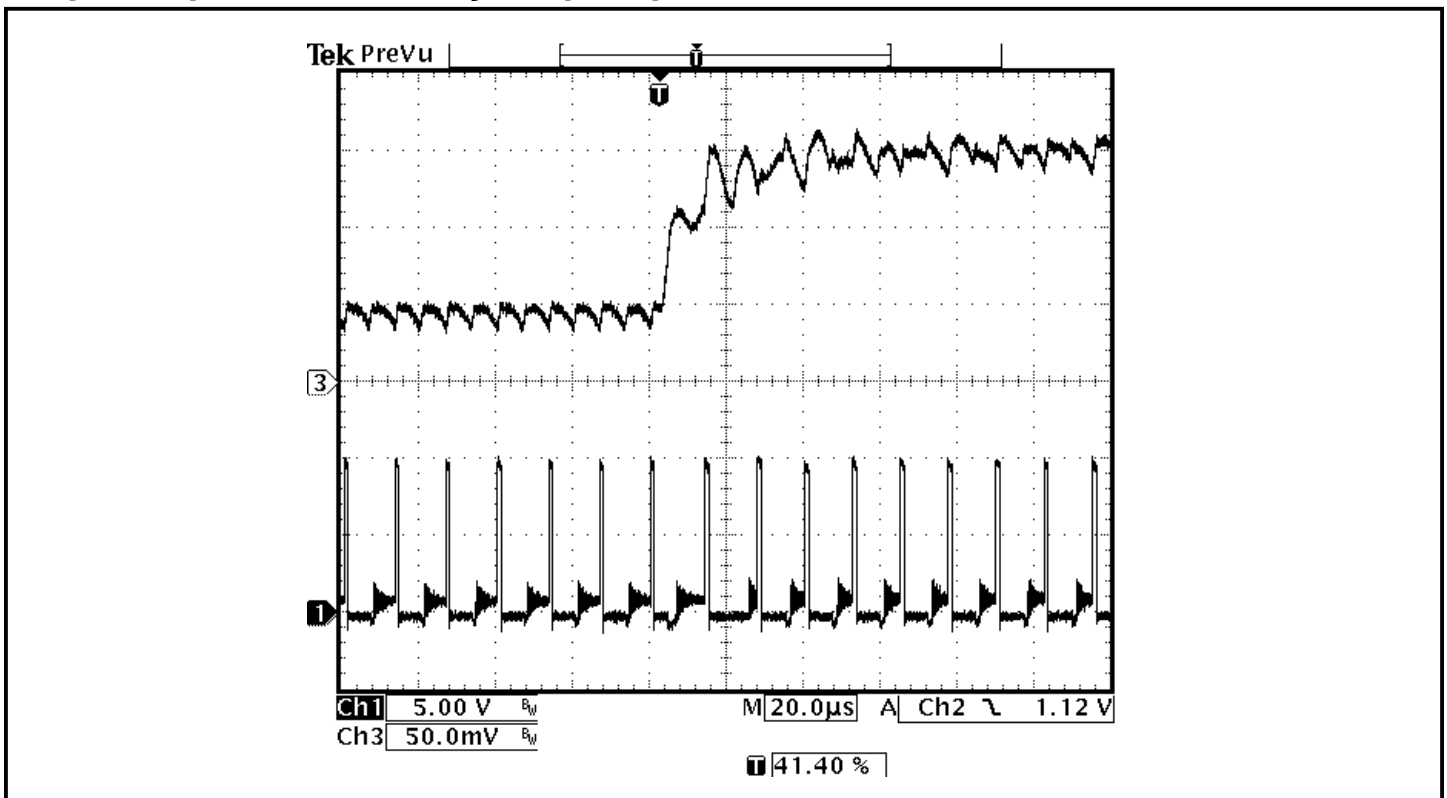
POWER MANAGEMENT

Typical Characteristics (Cont.)

Battery deepsleep mode to Deepsleep mode transition

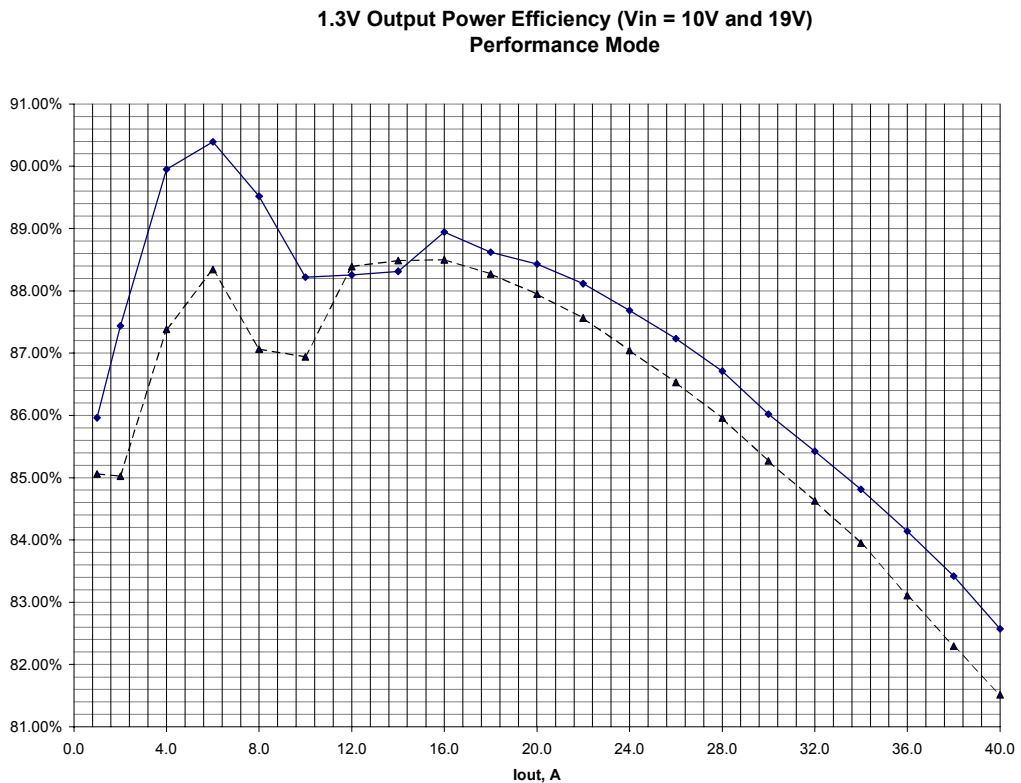
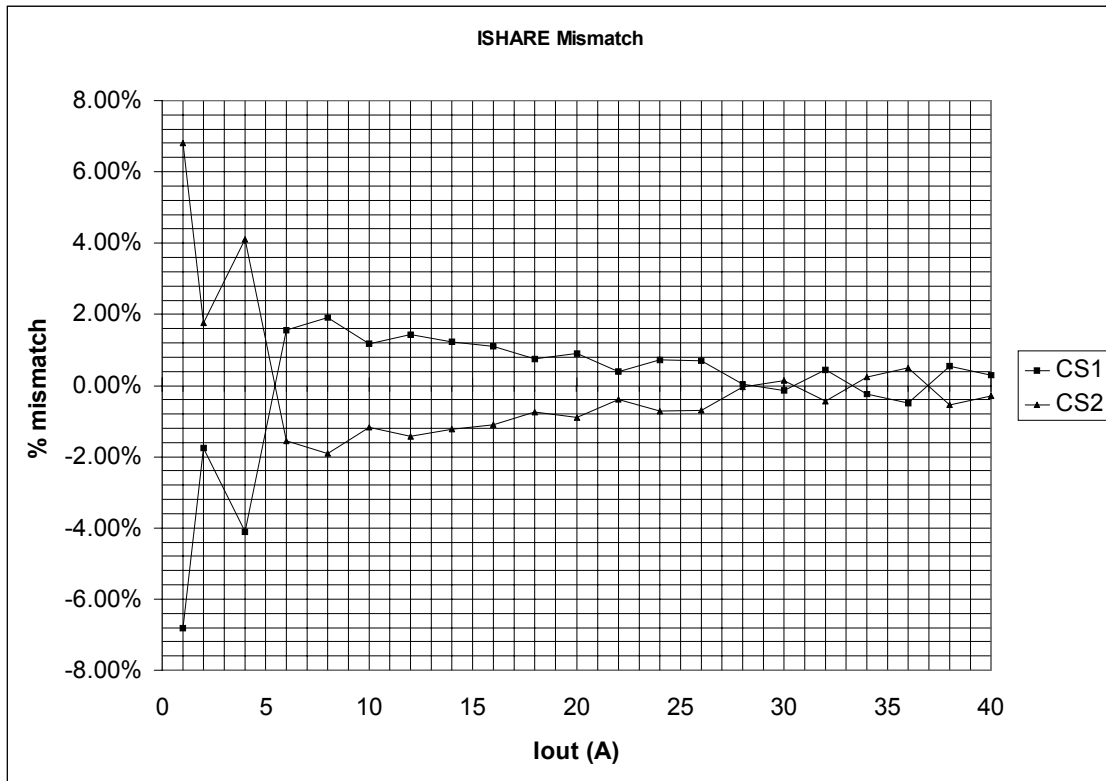


Deepsleep mode to Battery Deepsleep mode transition



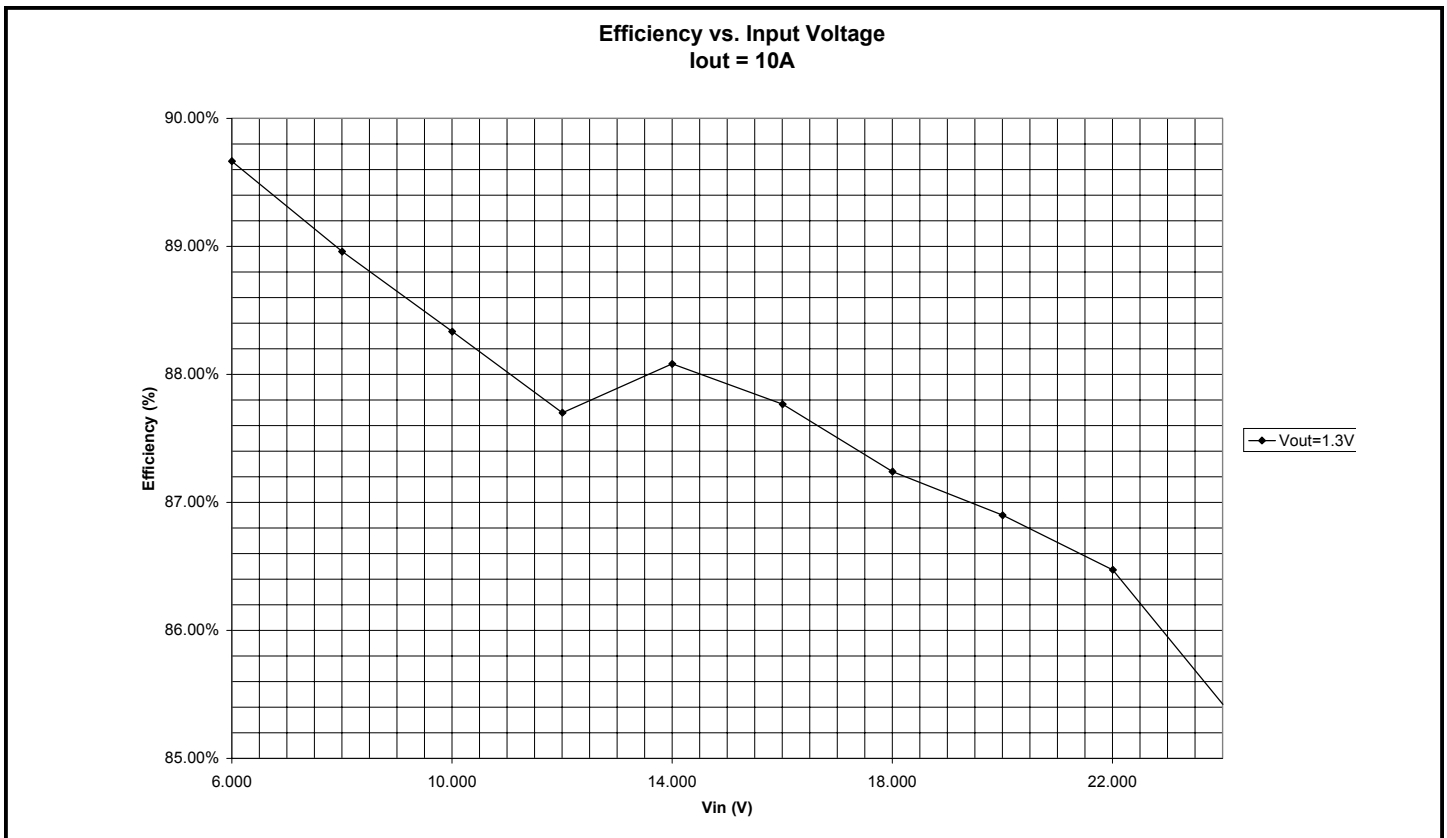
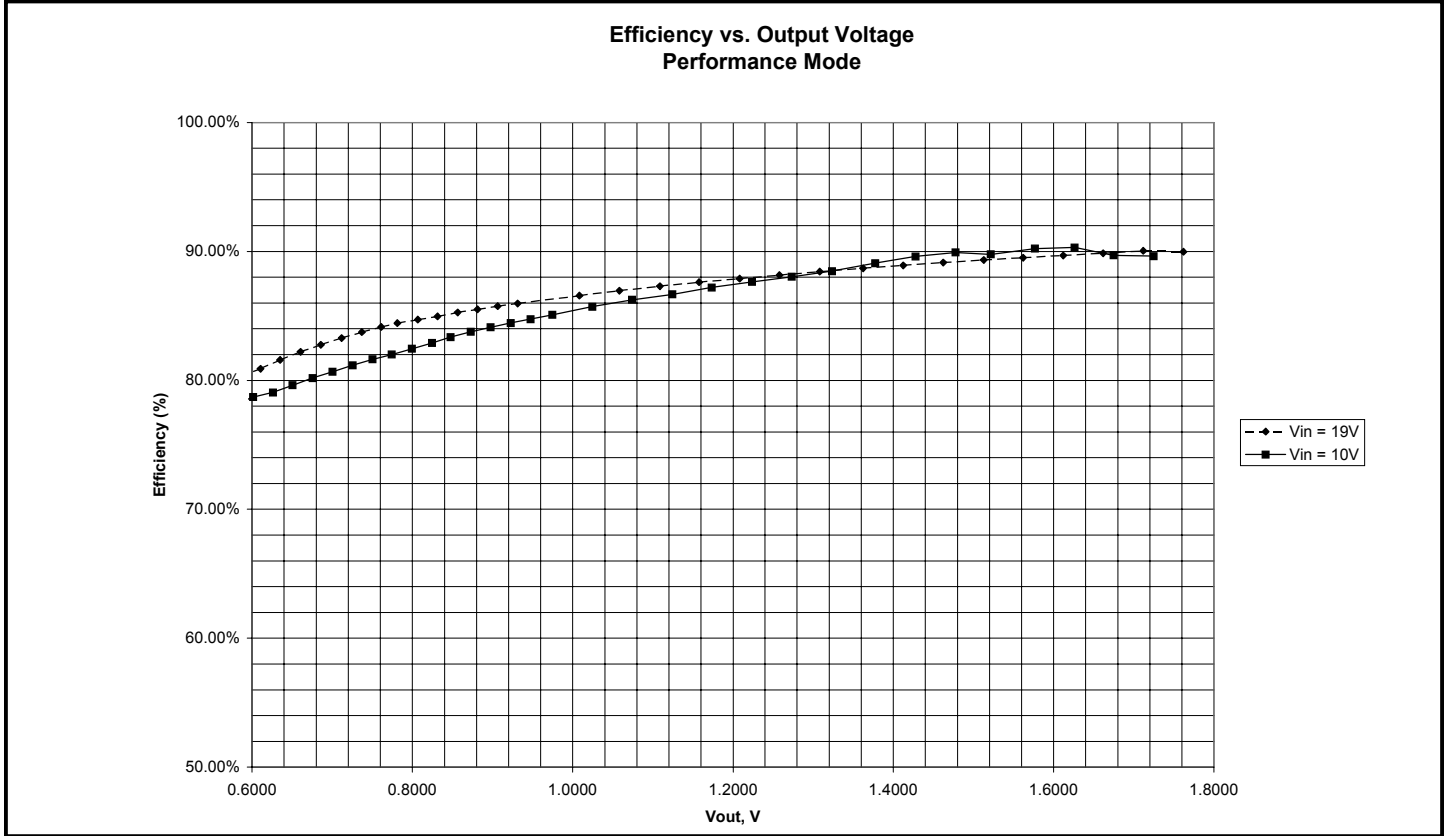
POWER MANAGEMENT

Typical Characteristics (Cont.)



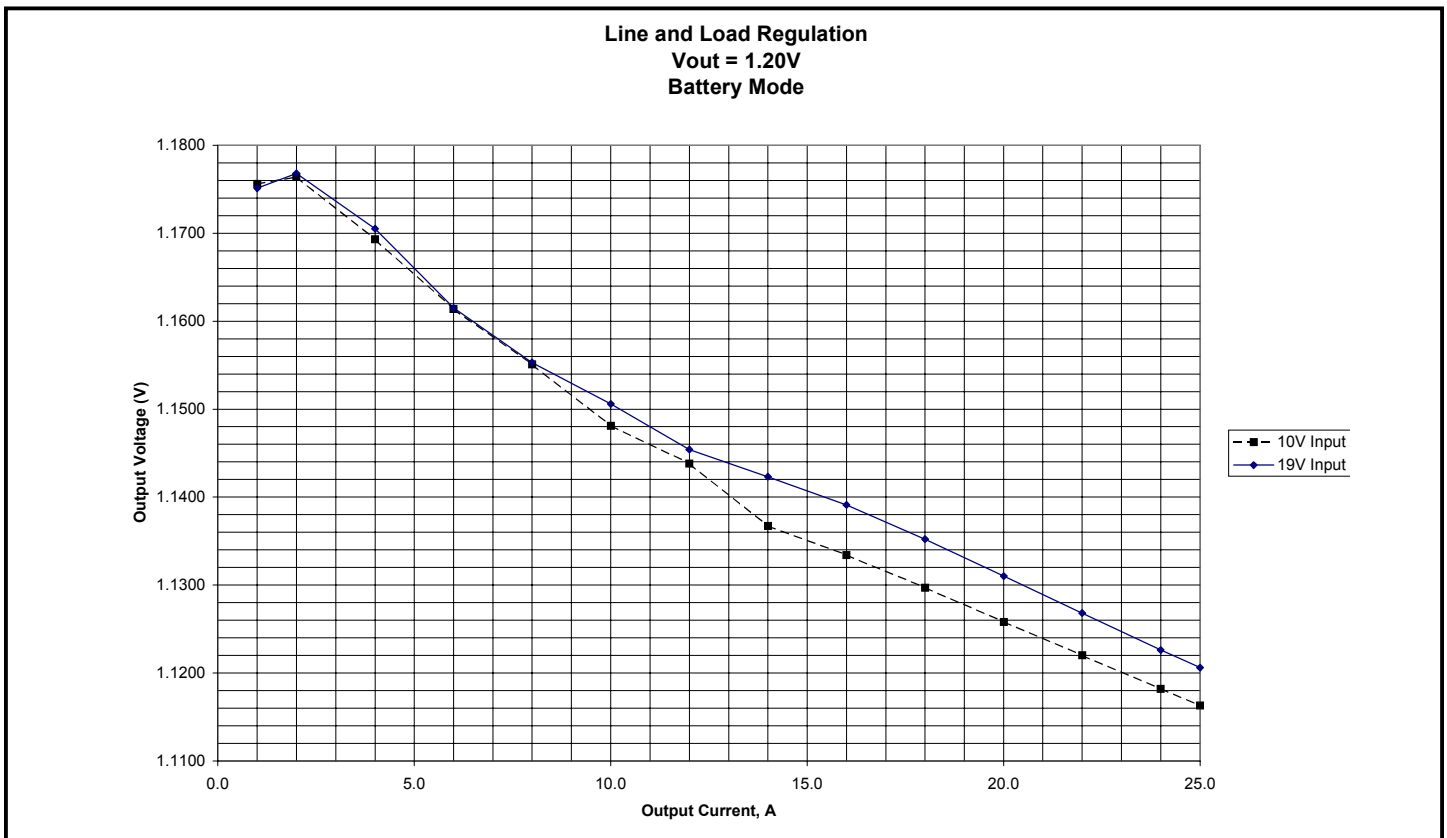
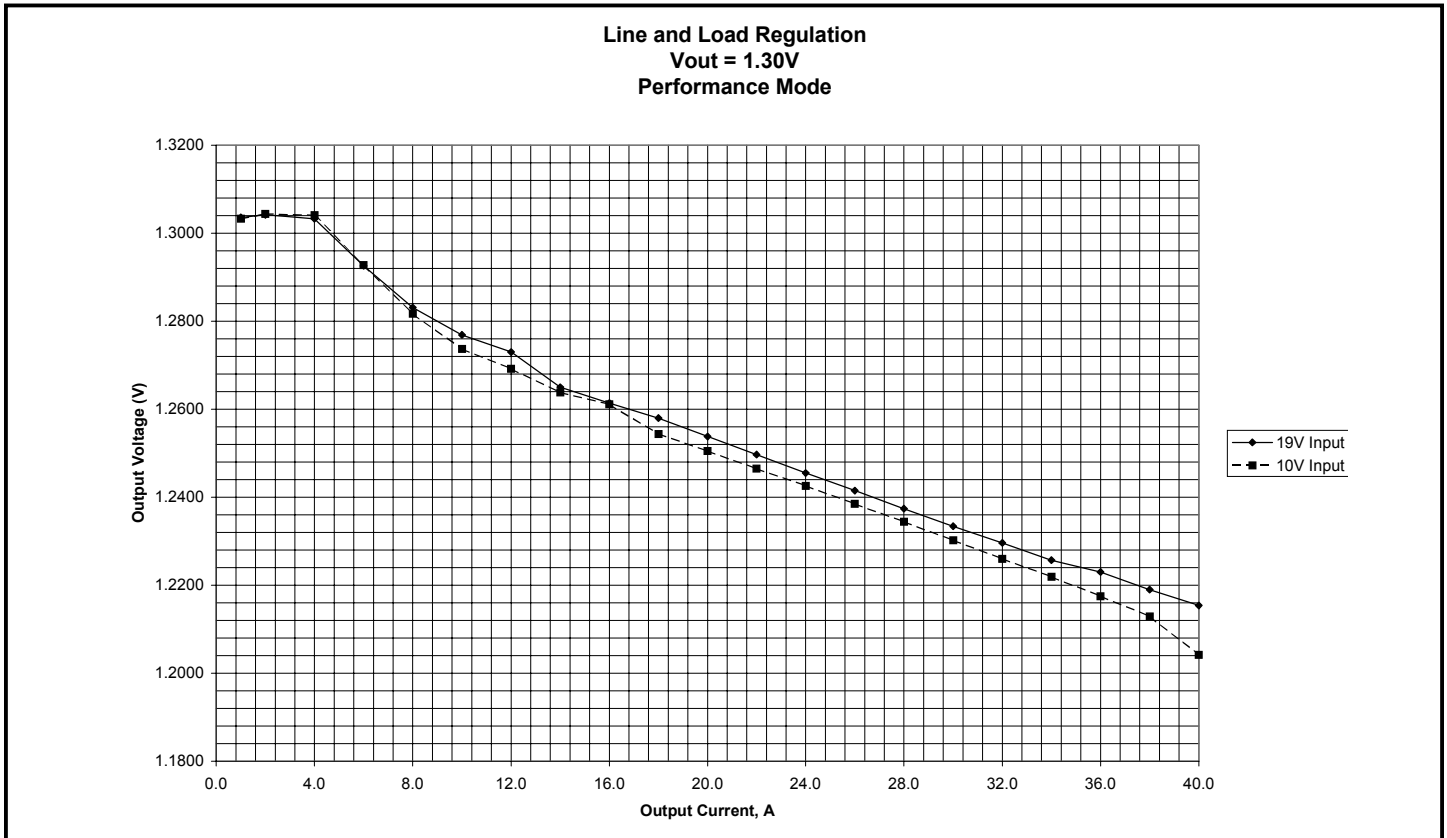
POWER MANAGEMENT

Typical Characteristics (Cont.)



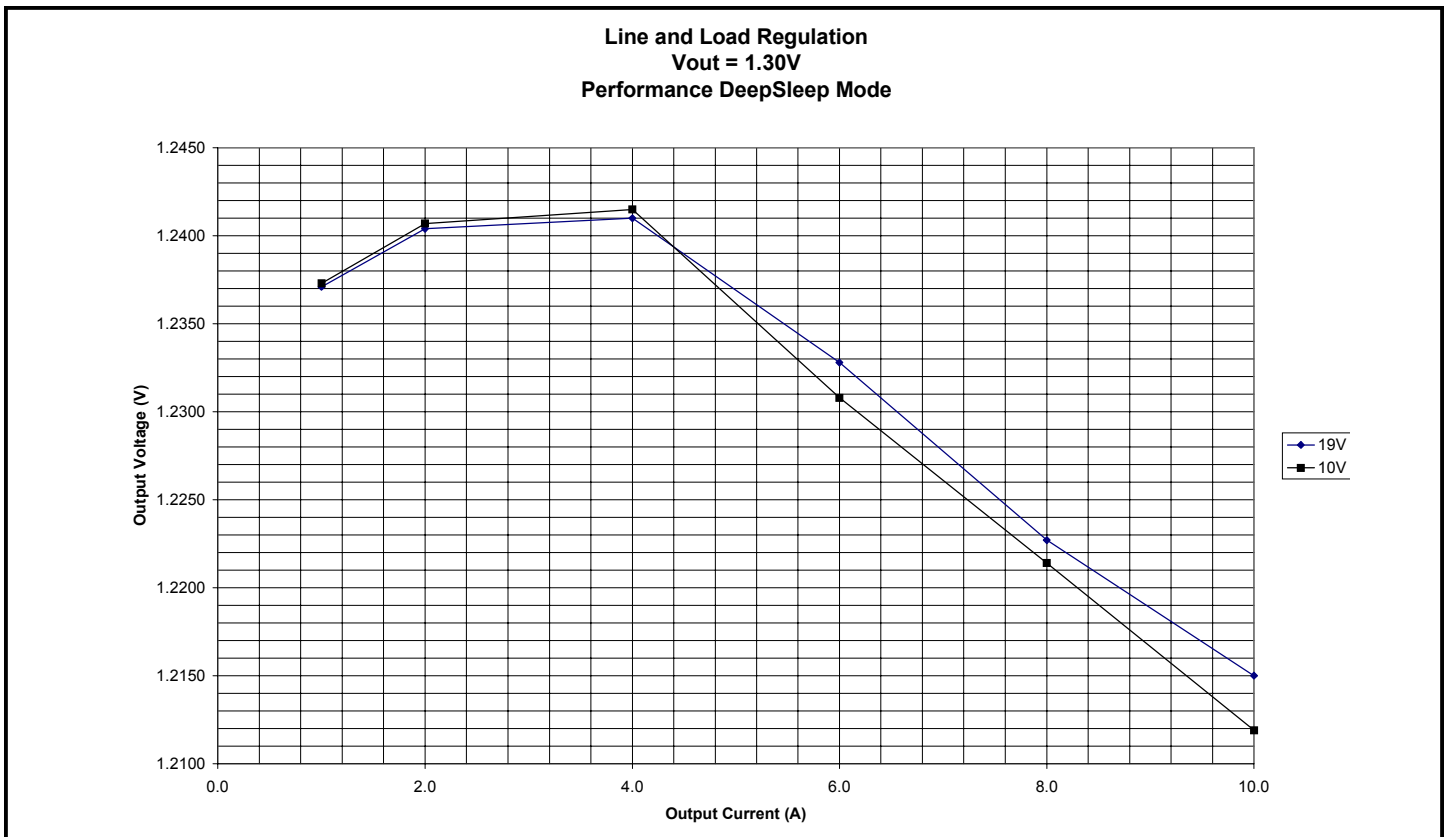
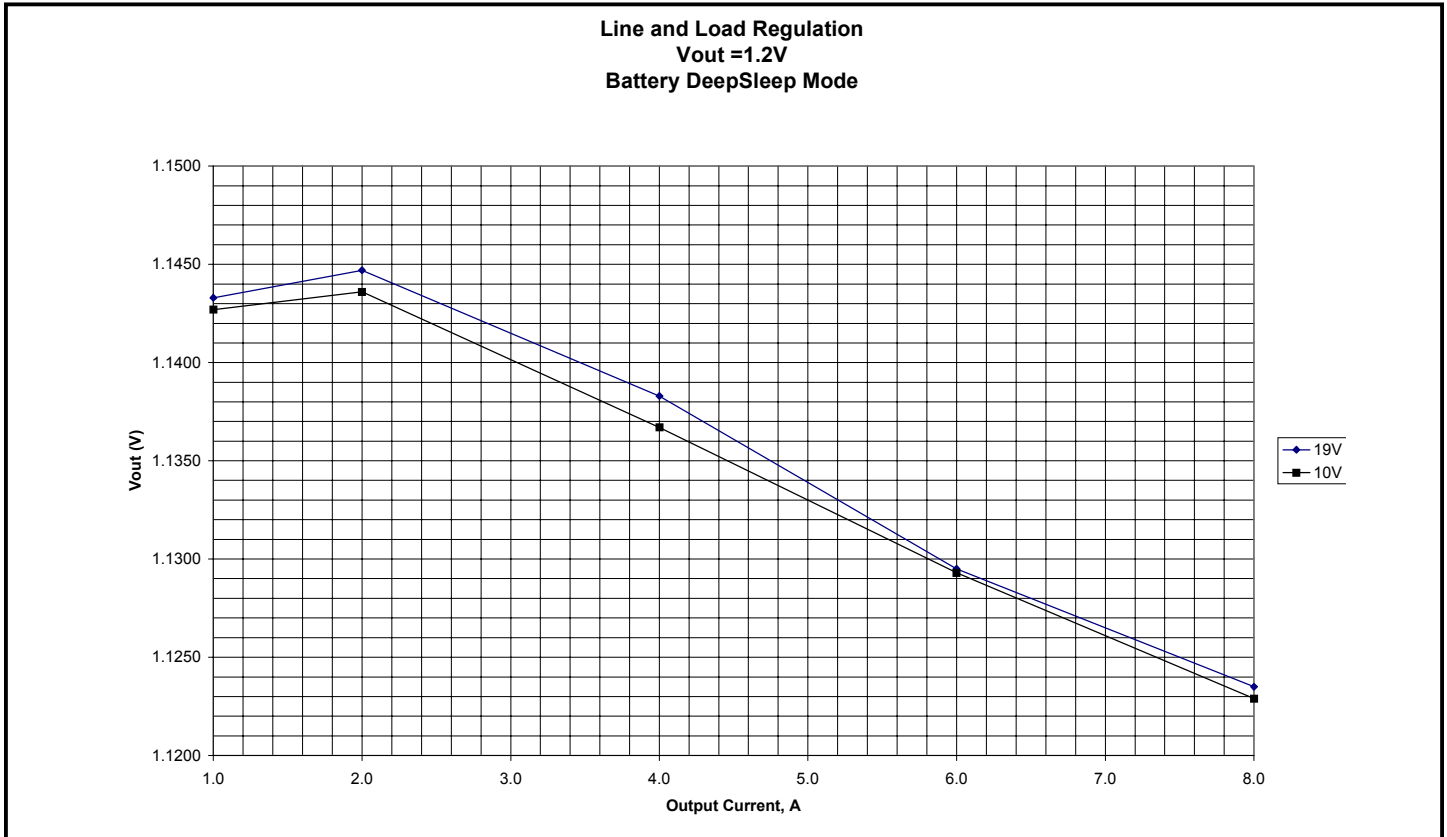
POWER MANAGEMENT

Typical Characteristics (Cont.)



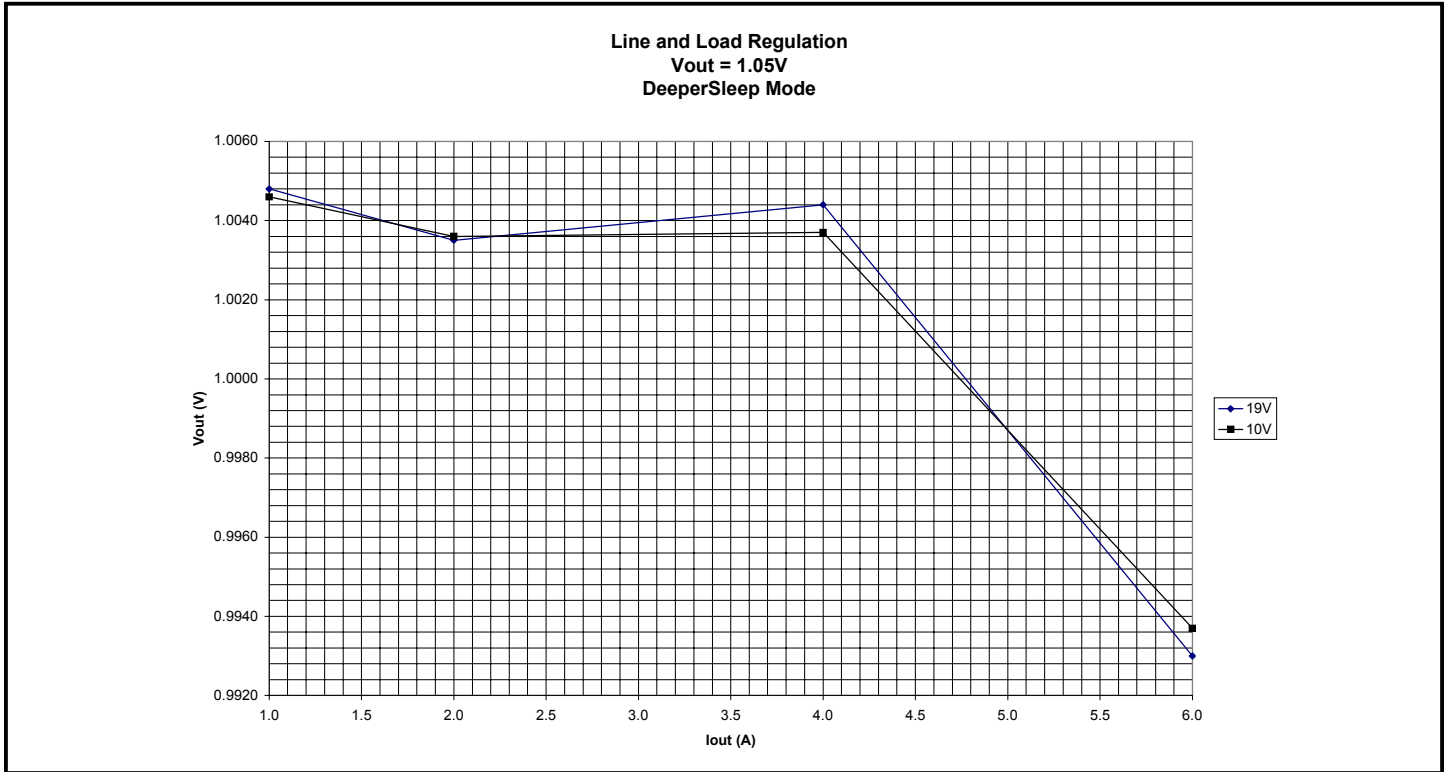
POWER MANAGEMENT

Typical Characteristics (Cont.)



POWER MANAGEMENT

Typical Characteristics (Cont.)



Outline Drawing - TSSOP-38

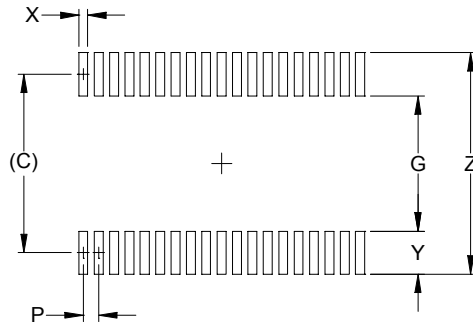
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.006	-	.010	0.17	-	0.27
c	.003	-	.007	0.09	-	0.20
D	.378	.382	.386	9.60	9.70	9.80
E1	.169	.173	.177	4.30	4.40	4.50
E	252 BSC			6.40 BSC		
e	.020 BSC			0.50 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	38			38		
theta1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION BD-1.

POWER MANAGEMENT

Land Pattern - TSSOP-38



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.020	0.50
X	.011	0.30
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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