Applications Note: SY8035
High Efficiency 5.5V, 5A, 1 MHz Synchronous Step Down Regulator
Preliminary Specification

General Description

SY8035 is a high-efficiency 1 MHz synchronous step-down DC-DC regulator IC capable of delivering up to 5A output current. SY8035 operates over a wide input voltage range from 2.7V to 5.5V and integrates the main switch and the synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction losses.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 1MHz switching frequency.

Ordering Information

SY8035 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package Type	Note
SY8035DBC	DFN3×3-10	

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 45/35mΩ
- Input voltage range: 2.7-5.5V
- 1 MHz switching frequency minimizes the external components
- External adjustable softstart limits the inrush current
- 100% dropout operation
- Power good indicator
- RoHS Compliant and Halogen Free
- Compact package: DFN3x3-10

Applications

- LCD TV
- Access Point Router
- Notebook PC
- Server

Typical Applications

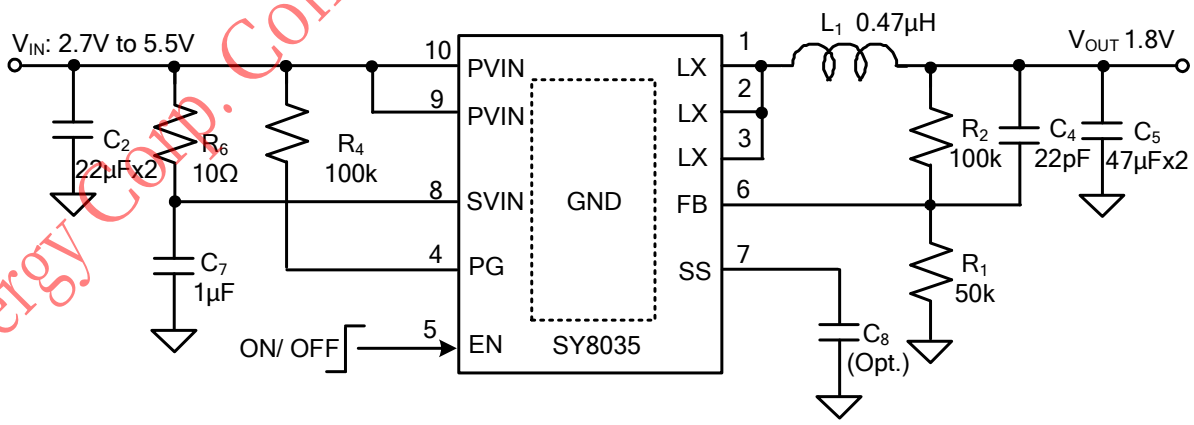
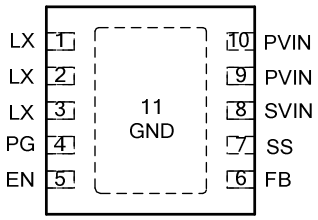


Figure 1: Typical application circuit diagram (V_{OUT}=1.8V)

Pinout (top view)



Top Mark: CX*xyz* (device code: CX, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
EN	5	Enable control. Pull high to turn on. Integrated 1MΩ pull-down resistor.
GND	11	Ground pin.
LX	1,2,3	Phase node pin. Connect this pin to the inductor.
SVIN	8	Signal power input pin. Decouple this pin to GND pin with at least 1μF ceramic cap.
PVIN	9,10	Power input pin. Decouple this pin to GND pin with at least 22μF ceramic cap.
FB	6	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$.
PG	4	Power good indicator(Open drain output). Low if the output < 90% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
SS	7	Softstart programming pin. Connect a capacitor from this pin to ground to program the softstart time. t_{SS}=Max(600μs, $C_{SS}\times0.6V/10\mu A$).

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 0.3V to 6.5V
Enable, FB Voltage---------- 0.3V to V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C DFN3X3-10 ---------- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 38°C/W
θ_{JC} ---------- 8°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V
Dynamic LX voltage in 50ns duration ---------- IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.7V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 0.47μH, C_{OUT} = 47μFx2, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF} · 105%		150		μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
PFET R_{ON}	$R_{DS(ON)-P}$			45		mΩ
NFET R_{ON}	$R_{DS(ON)-N}$			35		mΩ
PFET Current Limit	I_{LIM}		6			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.7	V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	F_{OSC}	I_{OUT}=1A		1		MHz
Min ON Time				80		ns
Max Duty Cycle			100			%
Thermal Shutdown Temperature	T_{SD}	Shutdown temperature		150		°C
		Hysteresis		10		
Soft Start Time	t_{SS}	C_{SS}=100nF		6		ms
		Without C_{SS}		0.6		
Phase Node Discharge Resistance	R_{DISCHG}			40		Ω

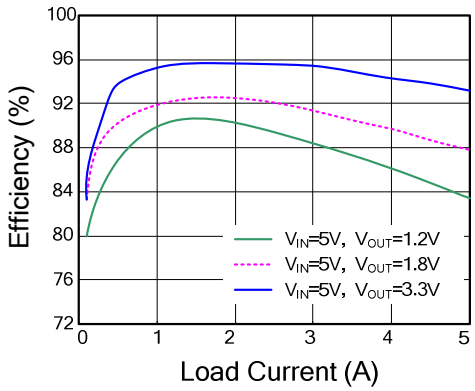
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

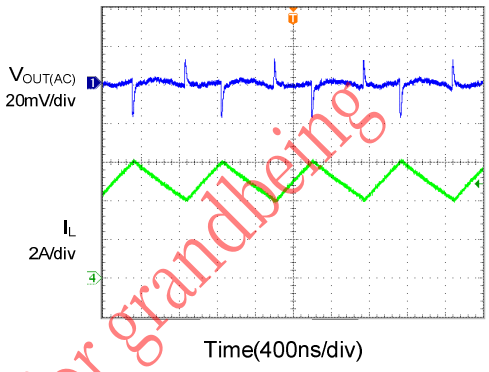
Typical Performance Characteristics

Efficiency vs. Load Current



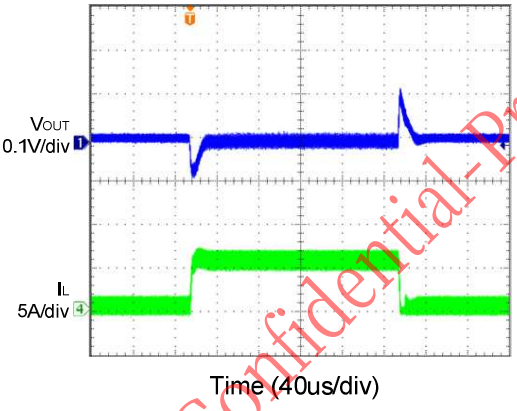
Output Ripple

(VIN=5V, VOUT=1.8V,Iload=5A)



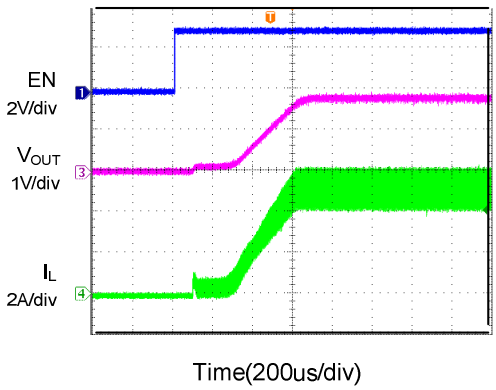
Load Transient

(VIN=5, VOUT=1.8V, Iload=0.5~5A)



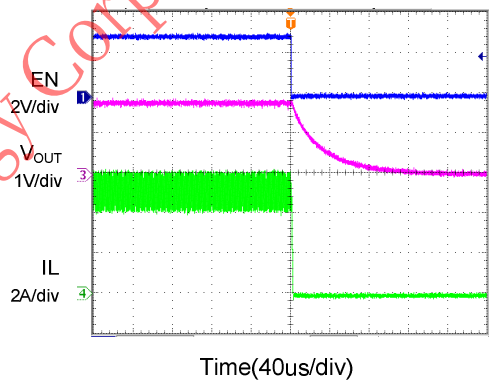
Startup

(VIN=5V, VOUT=1.8V,Iload=5A)

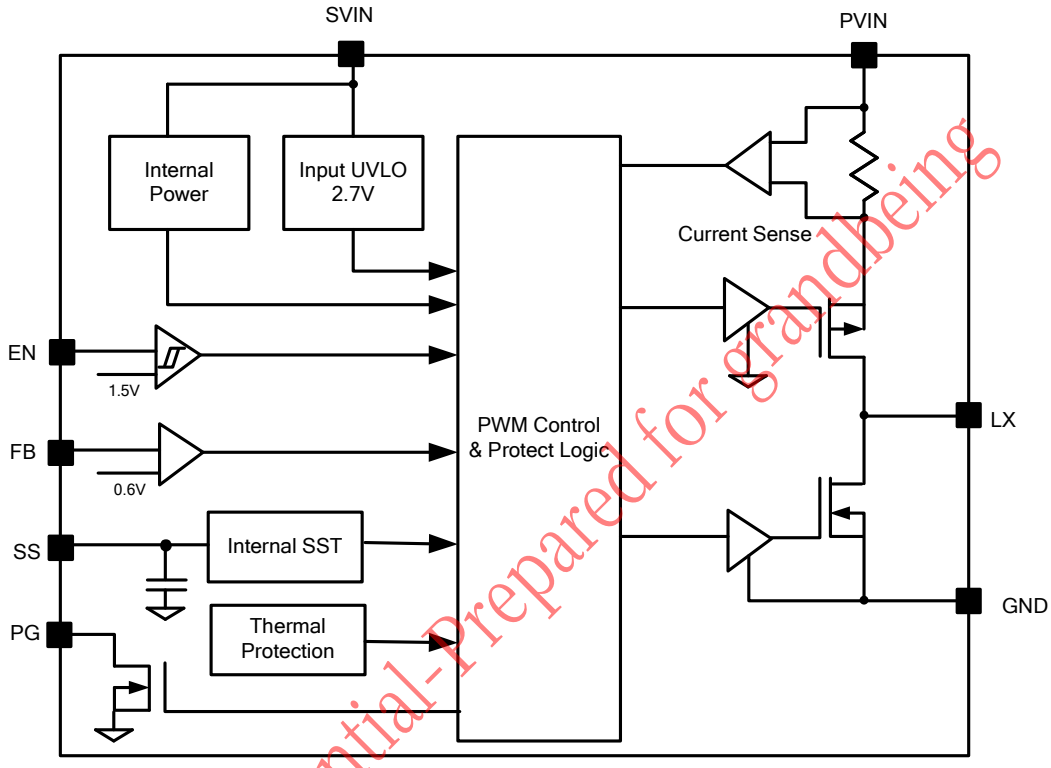


Shutdown

(VIN=5V, VOUT=1.8V,Iload=5A)



Block Diagram



Operation

SY8035 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching losses and conduction losses. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC achieves a higher efficiency with high switching frequency to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

SY8035 senses the output voltage conditions for the fault protection. If the DC output voltage is about 3% over the regulation level, both switches turn off and remain in the off state. If the DC output voltage is below 33% of the regulation level, the internal soft start node and the error amplifier output are discharged. The frequency is folded back to about 30% of the nominal frequency and the current limit is folded back to 5.0A to prevent the inductor current from runaway and to reduce the power dissipation of the IC under short circuit conditions.

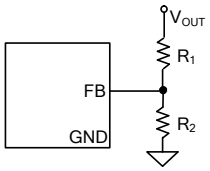
Applications Information

Because of the high integration in SY8035, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback resistor divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6} (\Omega)$$



Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)} \ (A)$$

This formula has a maximum at $V_{IN}=2\times V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$.

With the maximum load current at 5A, a typical X5R or better grade ceramic capacitor with 6.3V rating and more than two 22µF capacitors can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the PVIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and PVIN/GND pins.

A 1µF ceramic capacitor needs to be added across SVIN and GND.

Output capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than two 47µF capacitors.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY8035 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown, the SY8035 shutdown current drops to lower than 0.1μA, Driving the EN pin high (>1.5V) will turn on the IC again.

Power Good Indication

PG is an open-drain output pin. Connect an above 100k pull-up resistor to V_{IN}. PG pin will output high immediately after the output voltage exceeds 90% of normal output voltage.

Soft Start Programming

SY8035 provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by the external capacitor across SS pin and GND. The chip provides a 10μA charge current for the external capacitor. The soft start time is calculated as:

t_{SS}=MAX(600μS, C_{SS}×0.6V/10μA)

If a 0.1μF capacitor is used, the typical soft-start will be 6ms. If leaving SS pin floating, the internal soft-start time will be 0.6ms.

Load Transient Considerations:

SY8035 integrates the compensation components to achieve good stability and fast transient responses. Adding a 22pF~220pF ceramic capacitor in parallel with R_2 may further speed up the load transient responses.

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, L, R_1 and R_2.

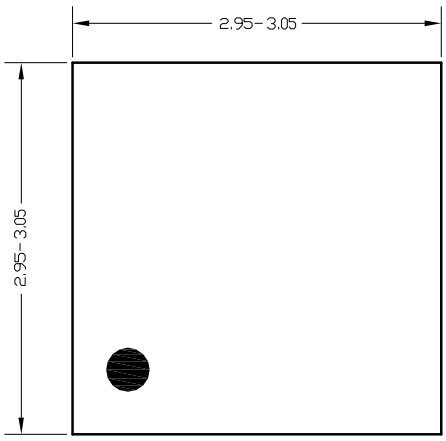
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. The center pad of SY8035 is used as the GND, so it is desirable to make a ground plane layer on a multi-layer board. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) The decoupling capacitor of PVIN and SVIN must be placed close enough to the pins. The loop area formed by the capacitors and GND must be minimized.

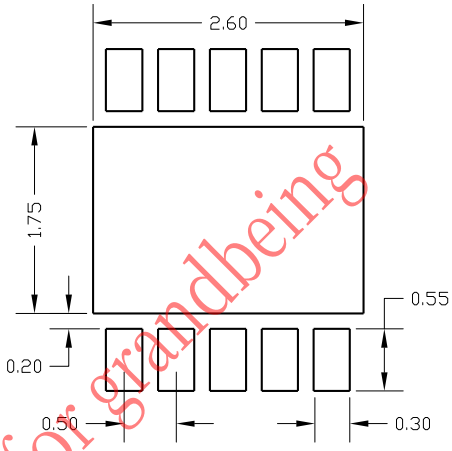
3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

4) The components R_1, R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

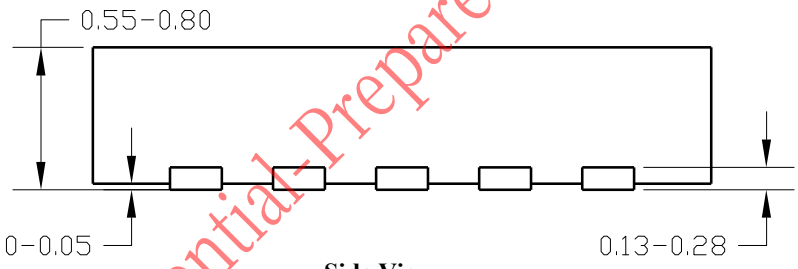
DFN3x3-10 Package outline



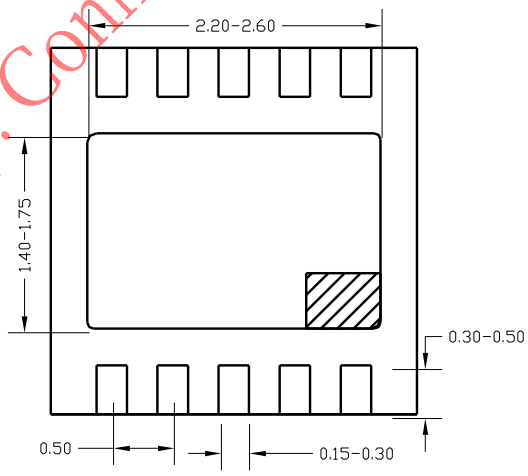
Top View

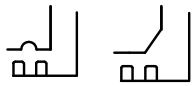


PCB layout (recommended)



Side View





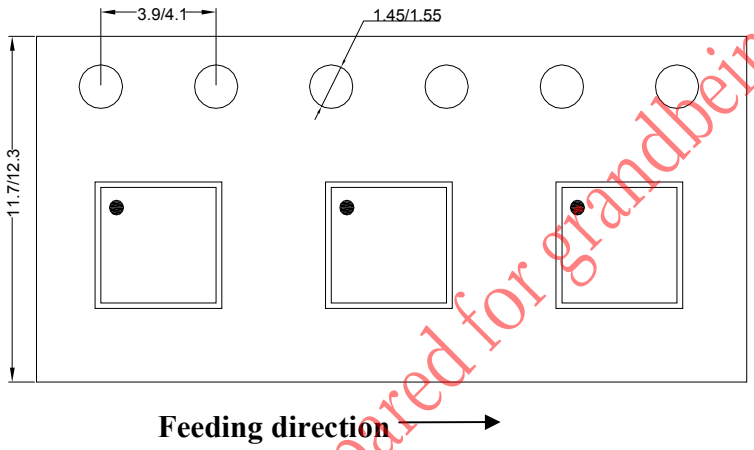
Detail A
Pin1 identifier: two options

Bottom View

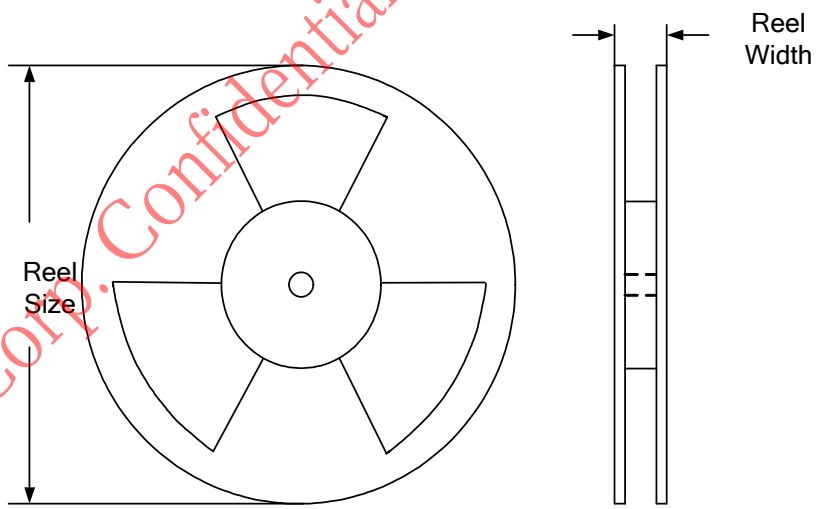
Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

Taping & Reel Specification

1. DFN3x3-10 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	12	8	13"	12.4	400	400	5000

3. Others: NA